Design Project Figures

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Schematics and Symbols

2bit Adder

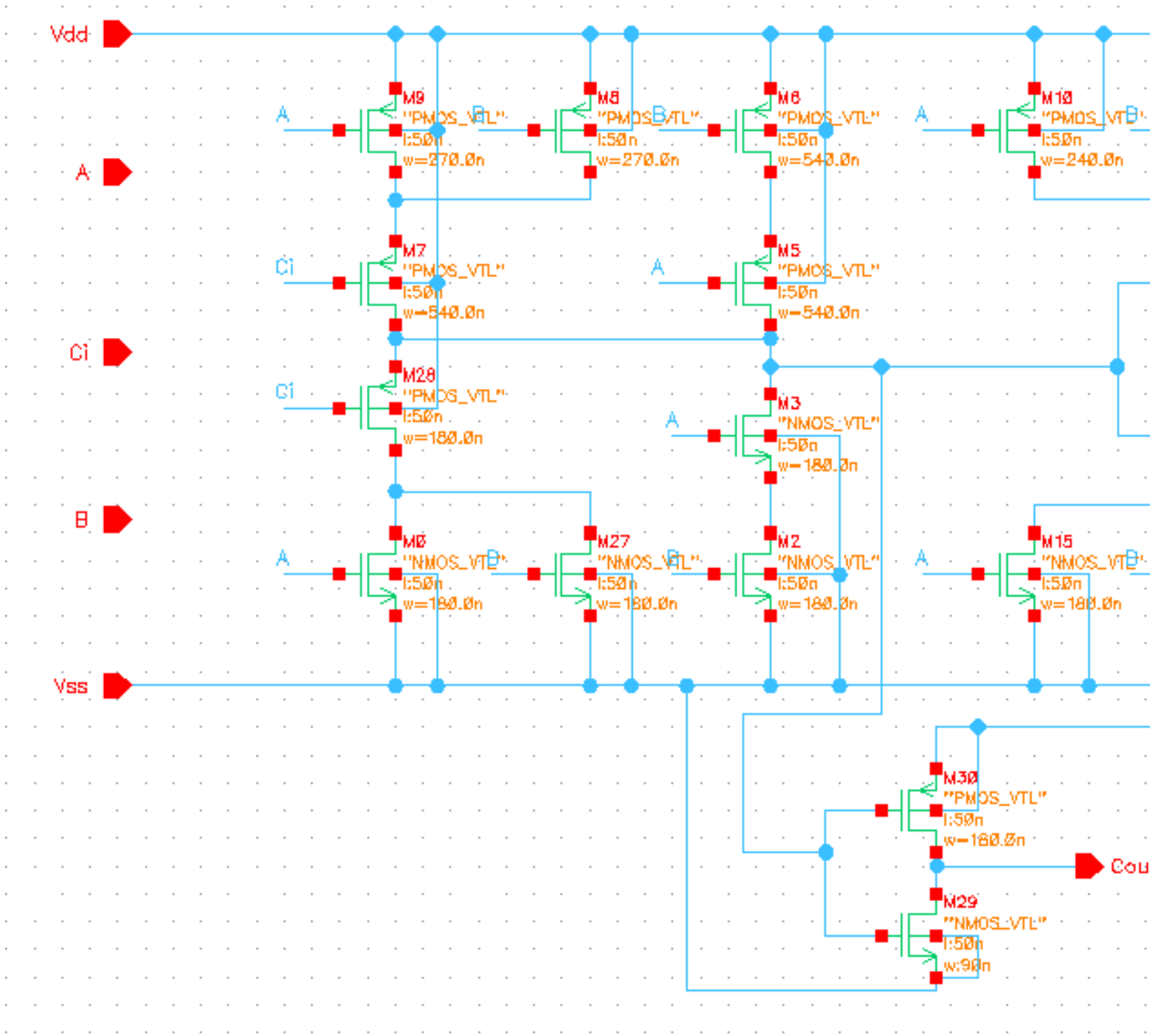

Figure 1 – 2 Bit Adder Schematic (Part 1 – Left side)

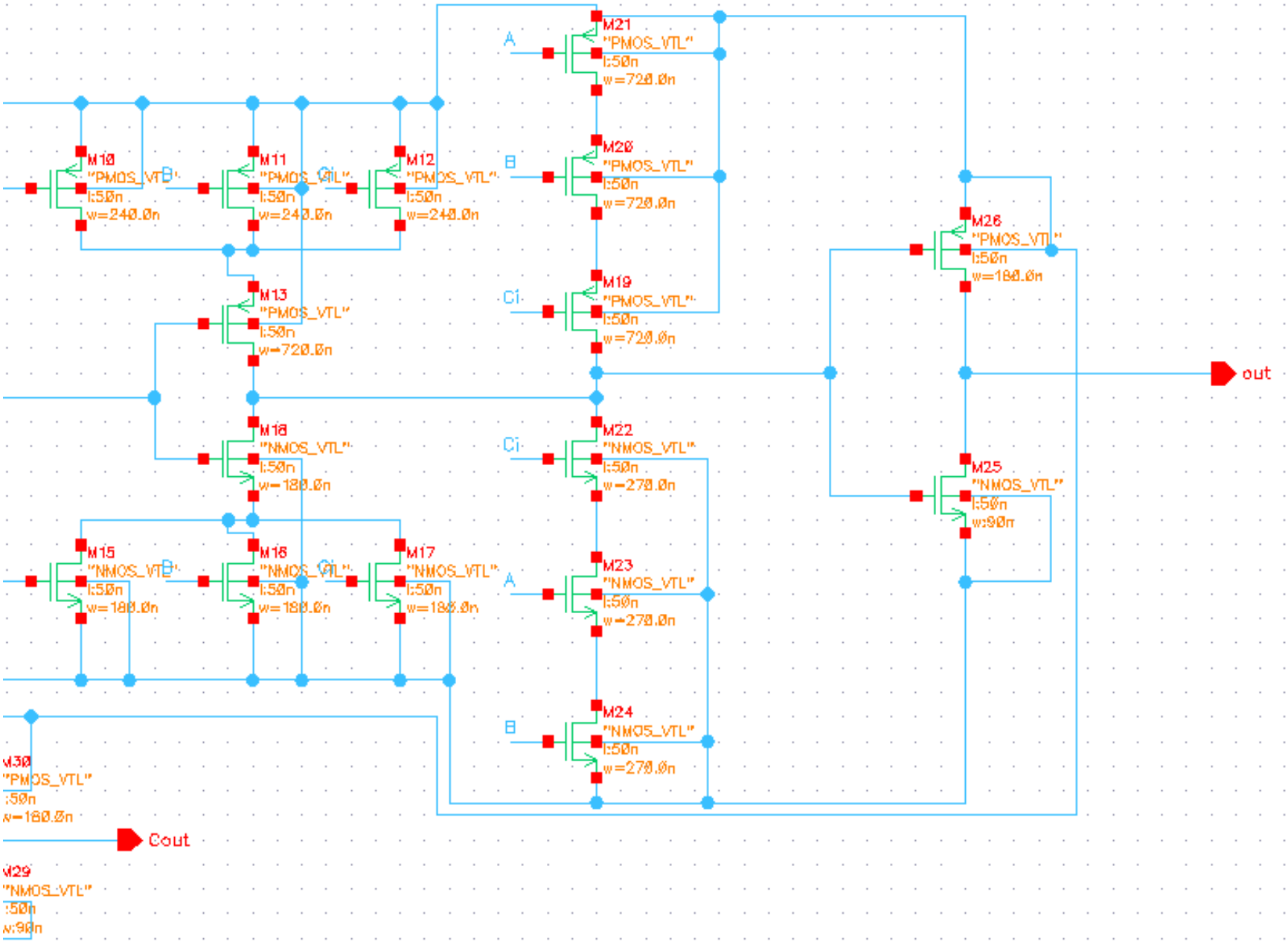

Figure 2 - 2 Bit Adder Schematic (Part 2 - Right side)

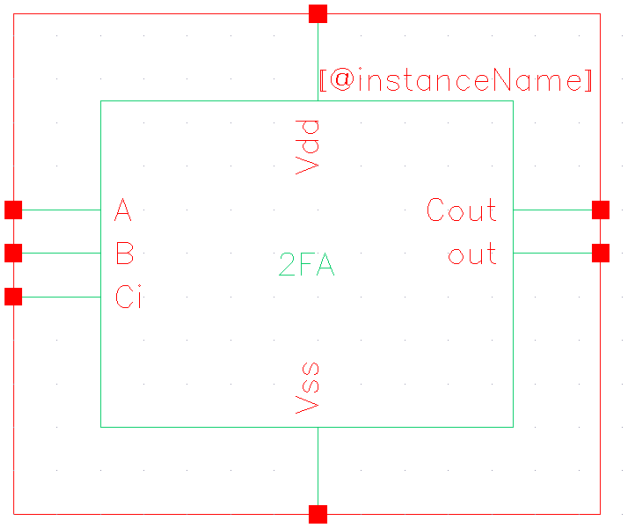

Figure 3- 2 Bit Adder Symbol

8bit Adder

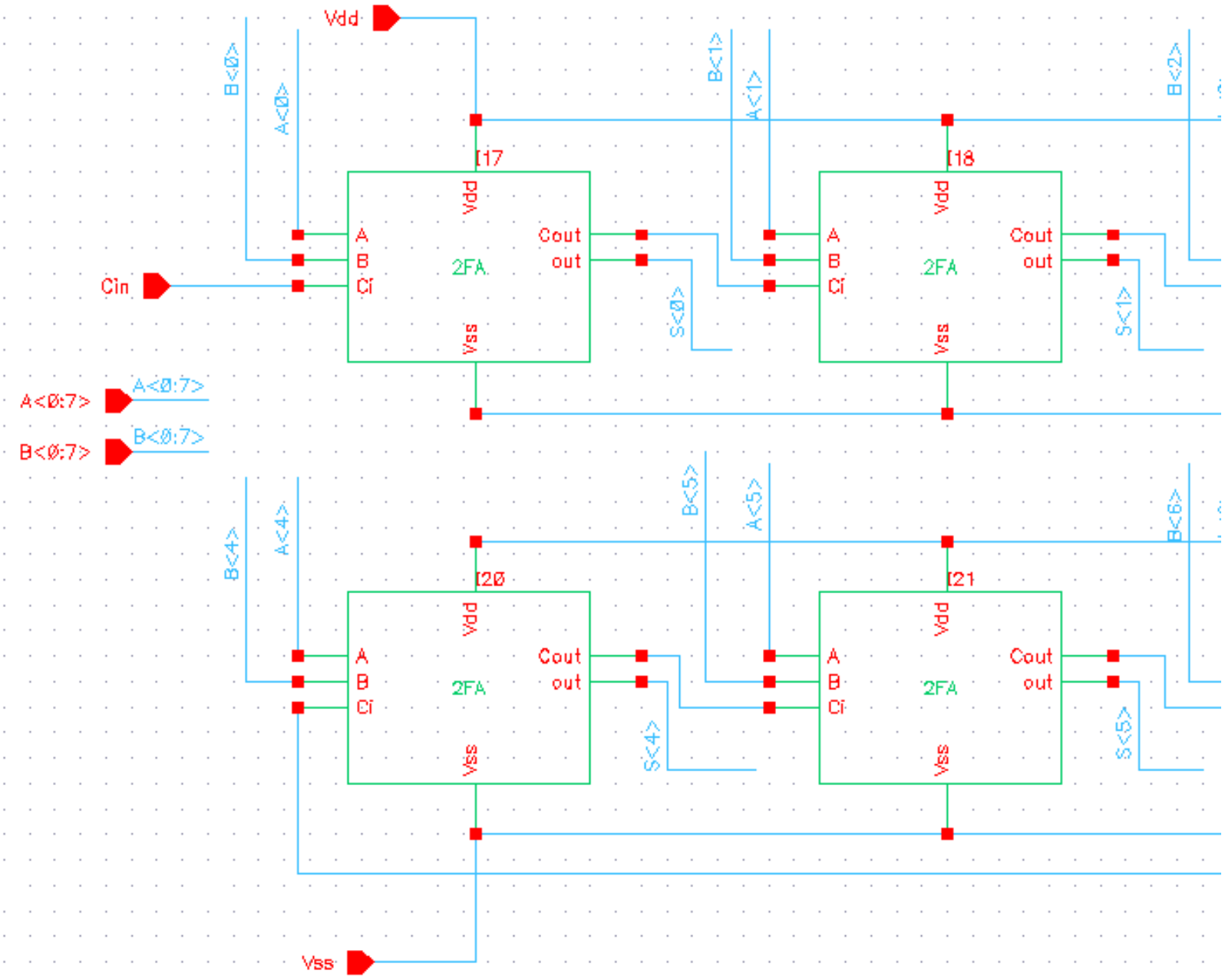

Figure 4 - 8 Bit Adder Schematic (Part 1 – Left side)

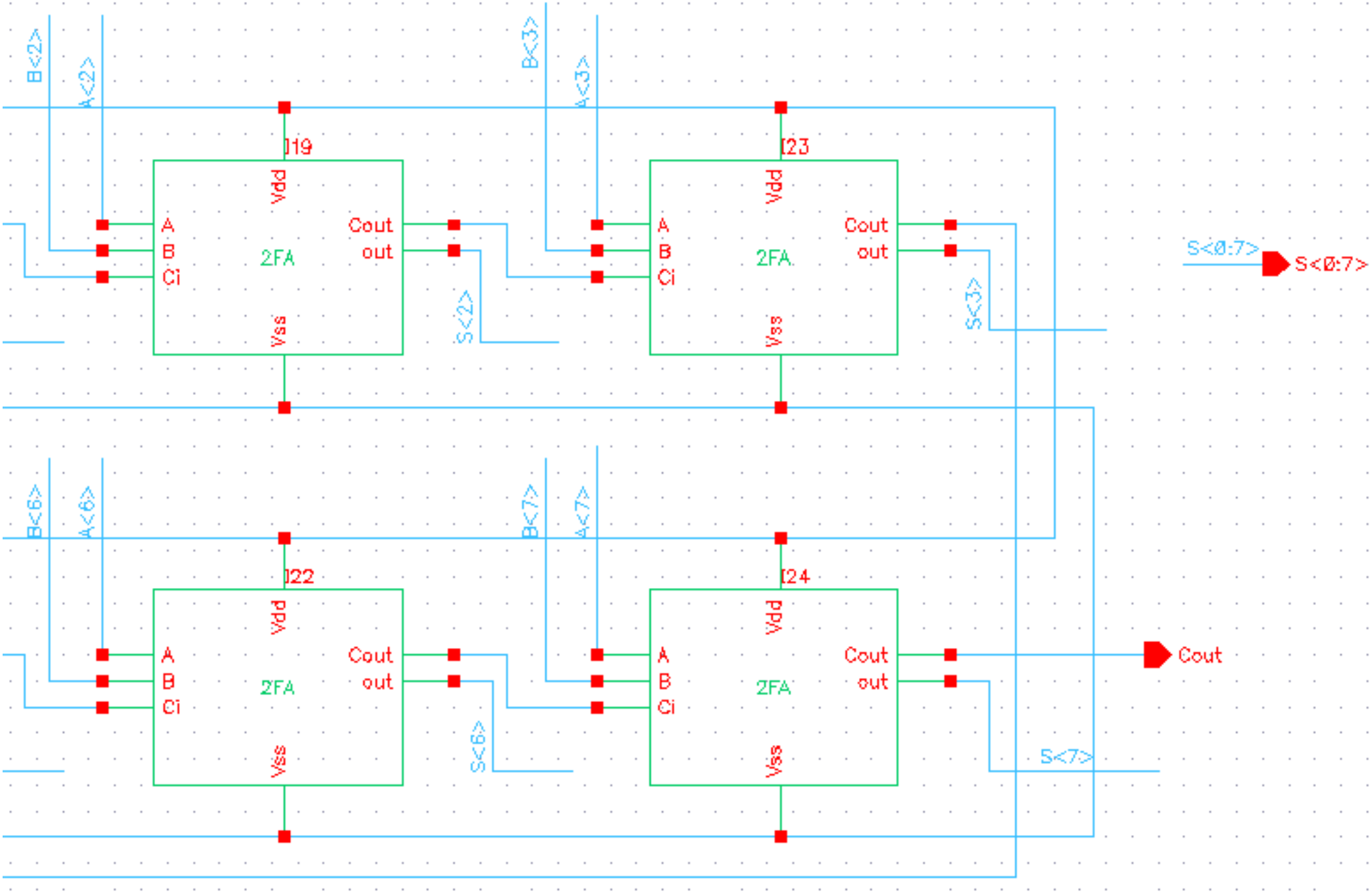

Figure 5 - 2 Bit Adder Schematic (Part 2 – Right side)

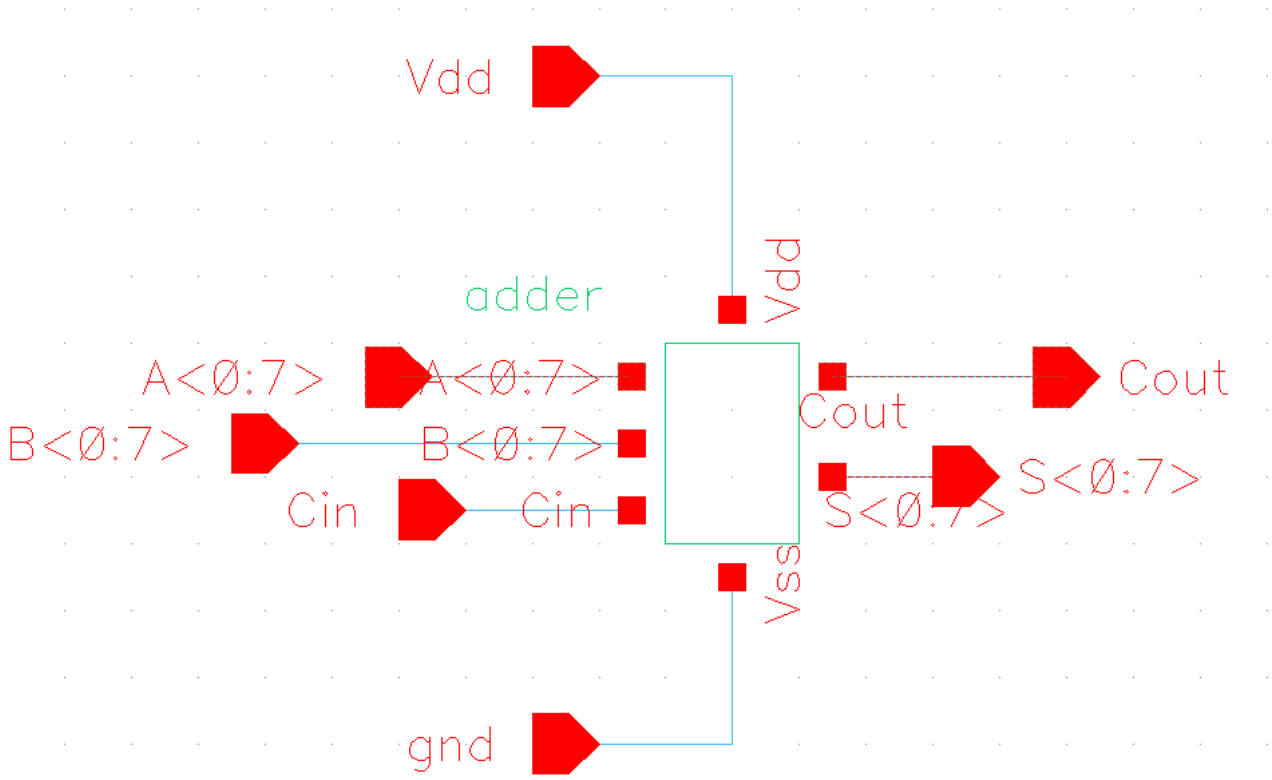

Figure 6 – 8 Bit Adder Symbol

XOR

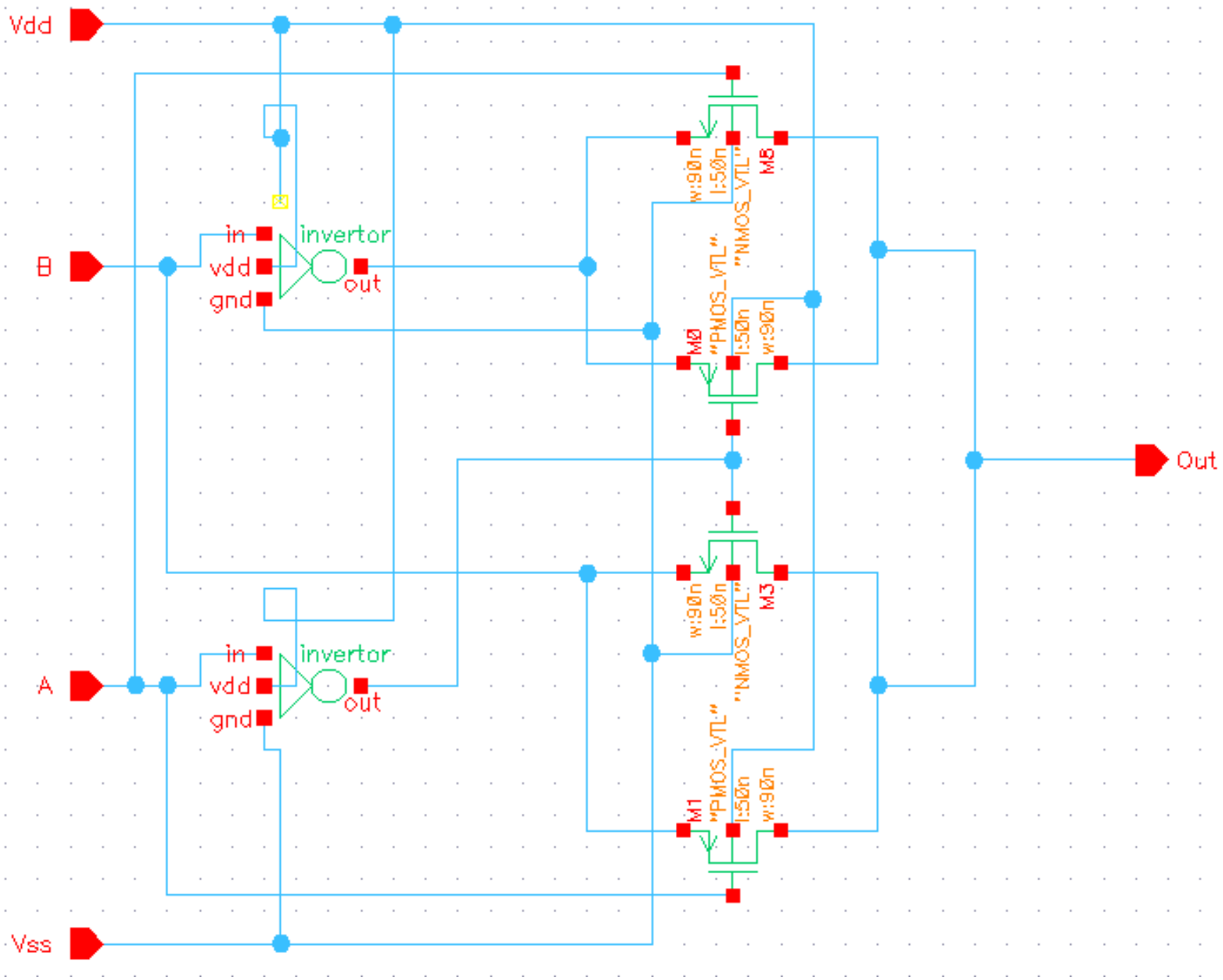

Figure 7 – XOR Schematic

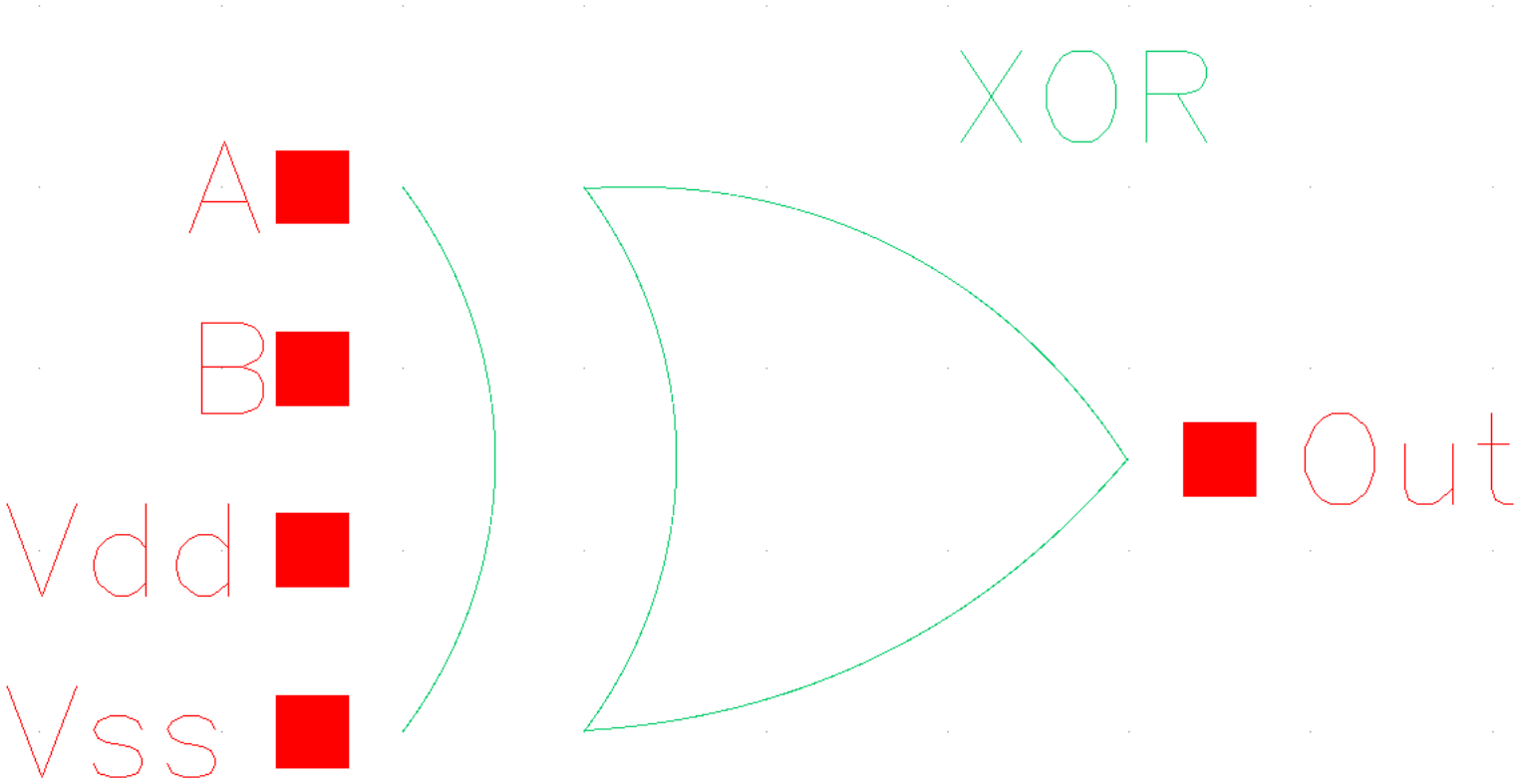

Figure 8 – XOR Symbol

AND (from NAND gate)

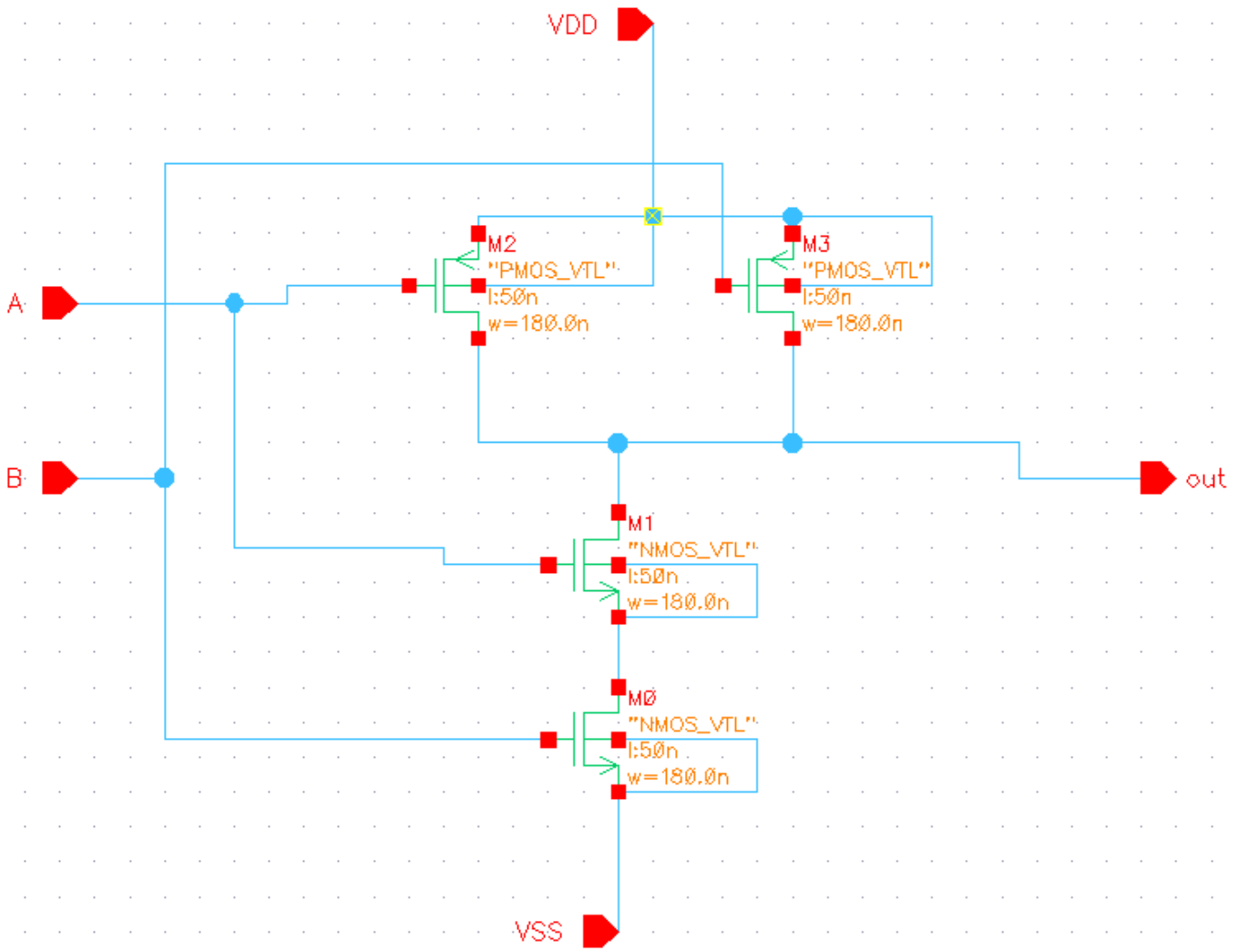

Figure 9 – NAND Schematic

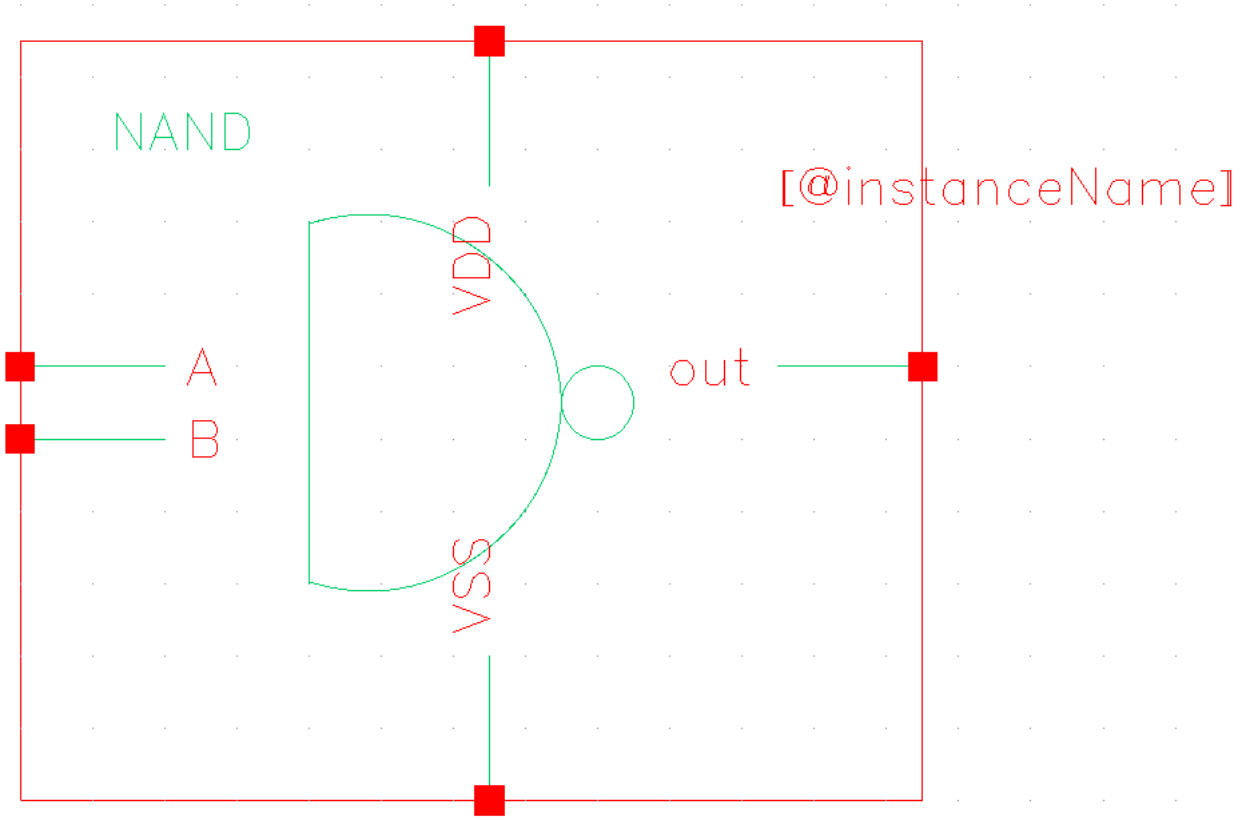

Figure 10 – NAND Symbol

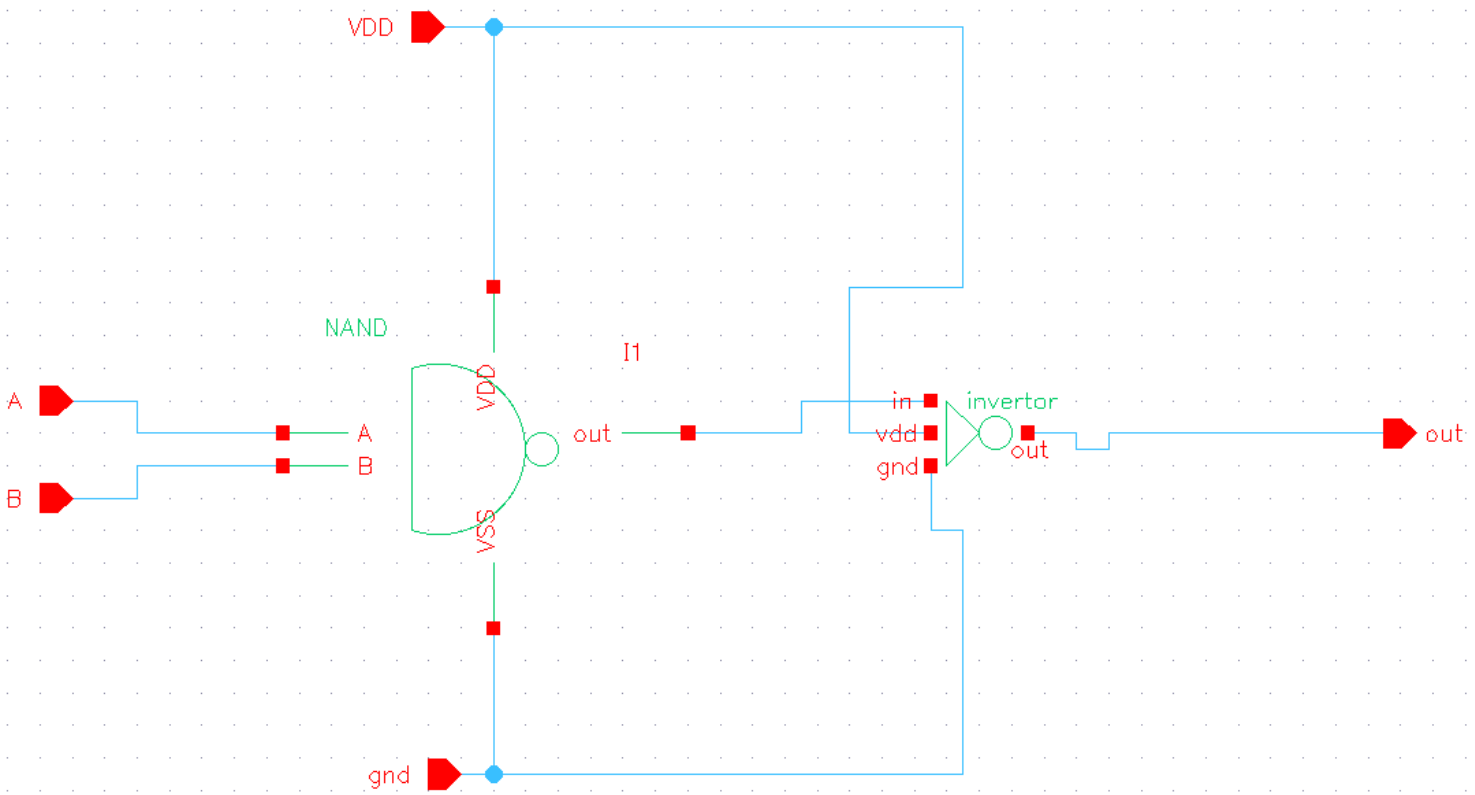

Figure 11 – AND Schematic (using NAND)

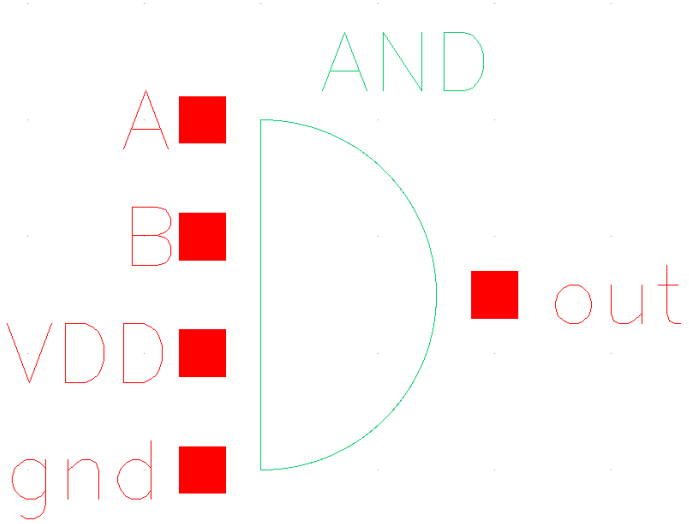

Figure 12 – AND Symbol

OR

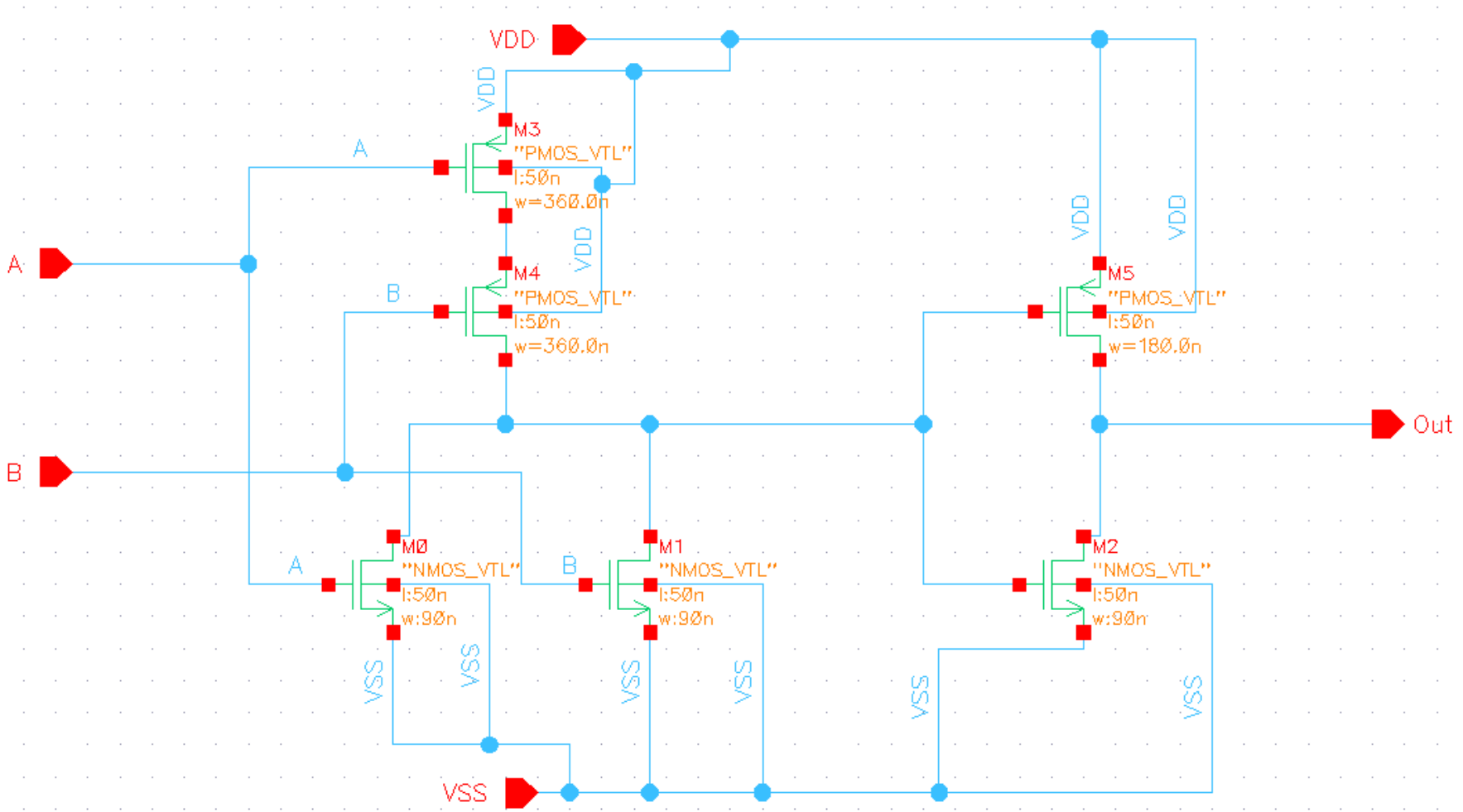

Figure 13 – OR Schematic

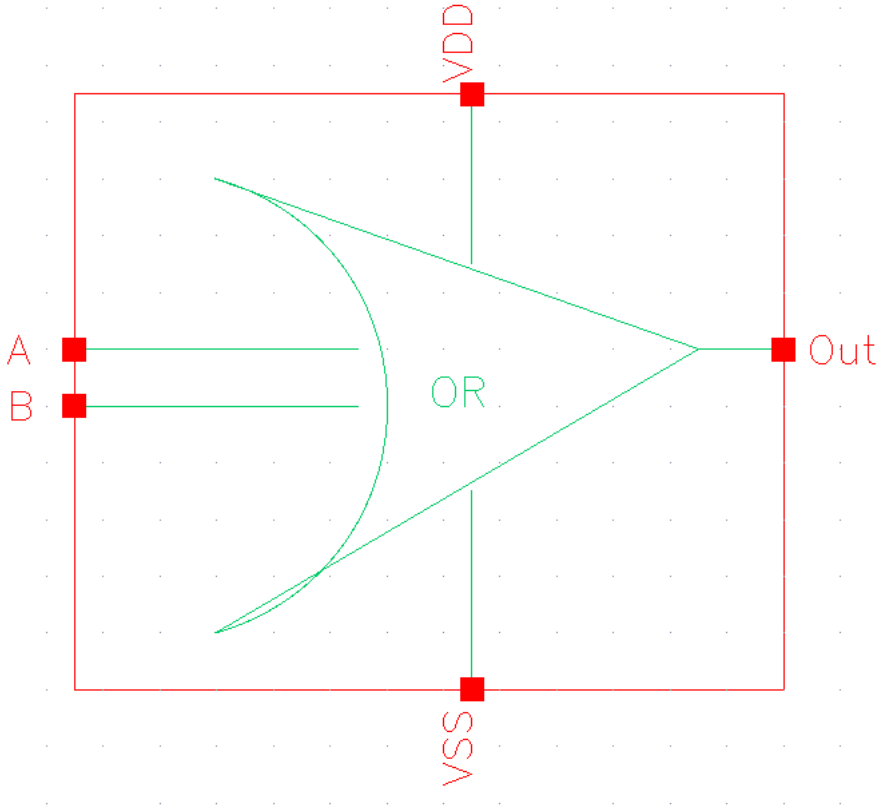

Figure 14 – OR Symbol

Transmission Gate

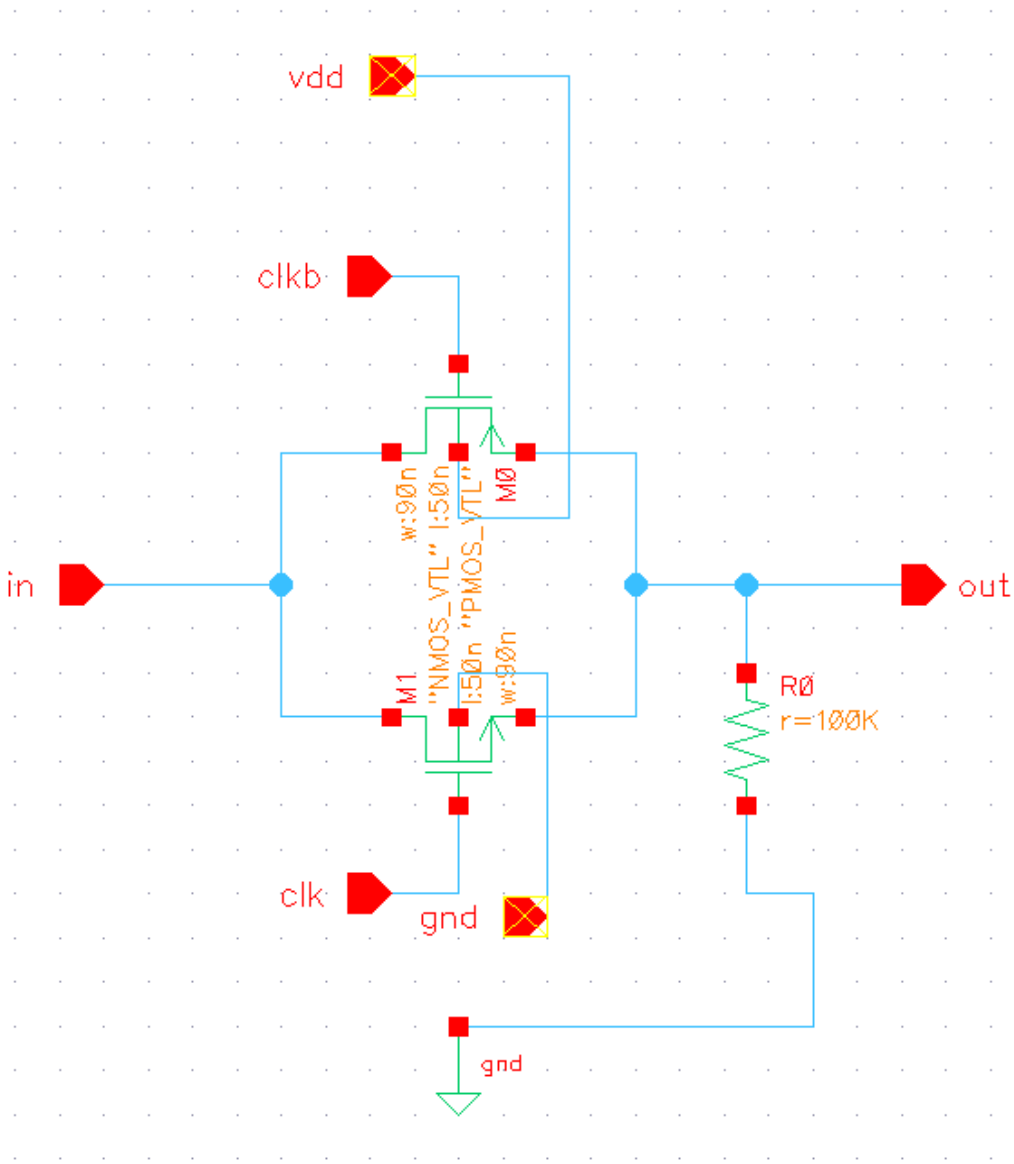

Figure 15 – Transmission Gate Schematic

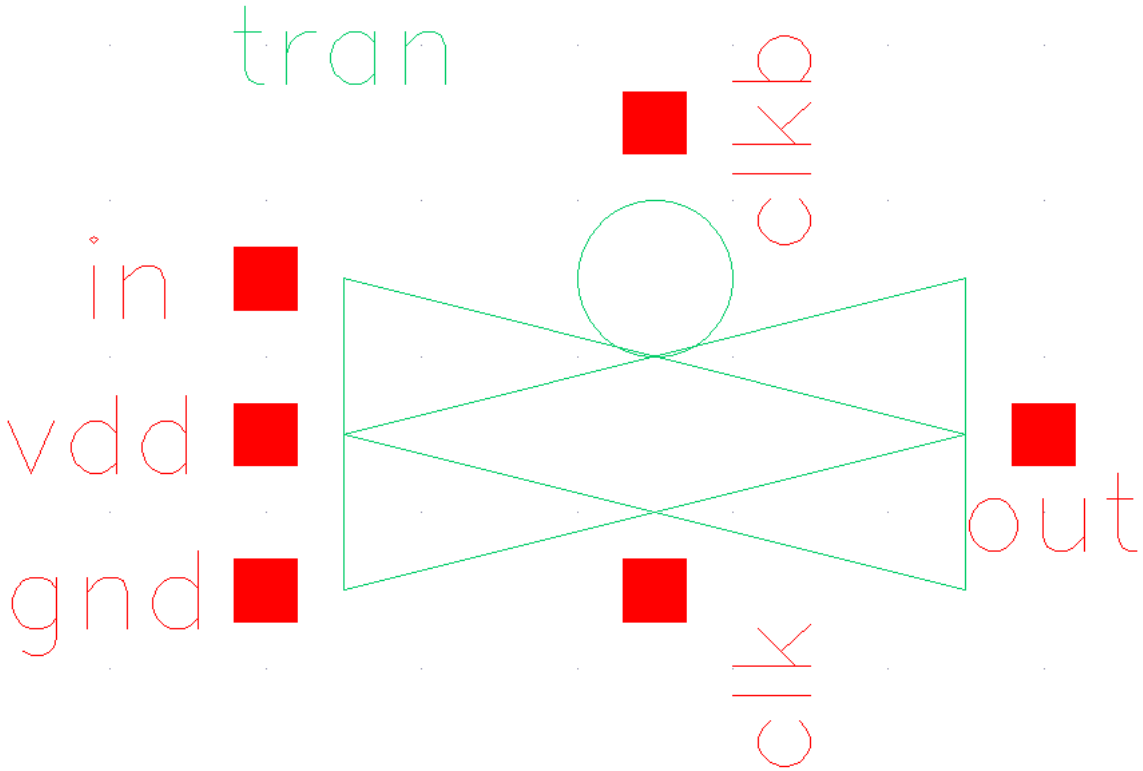

Figure 16 – Transmission Gate Symbol

8to1 MUX

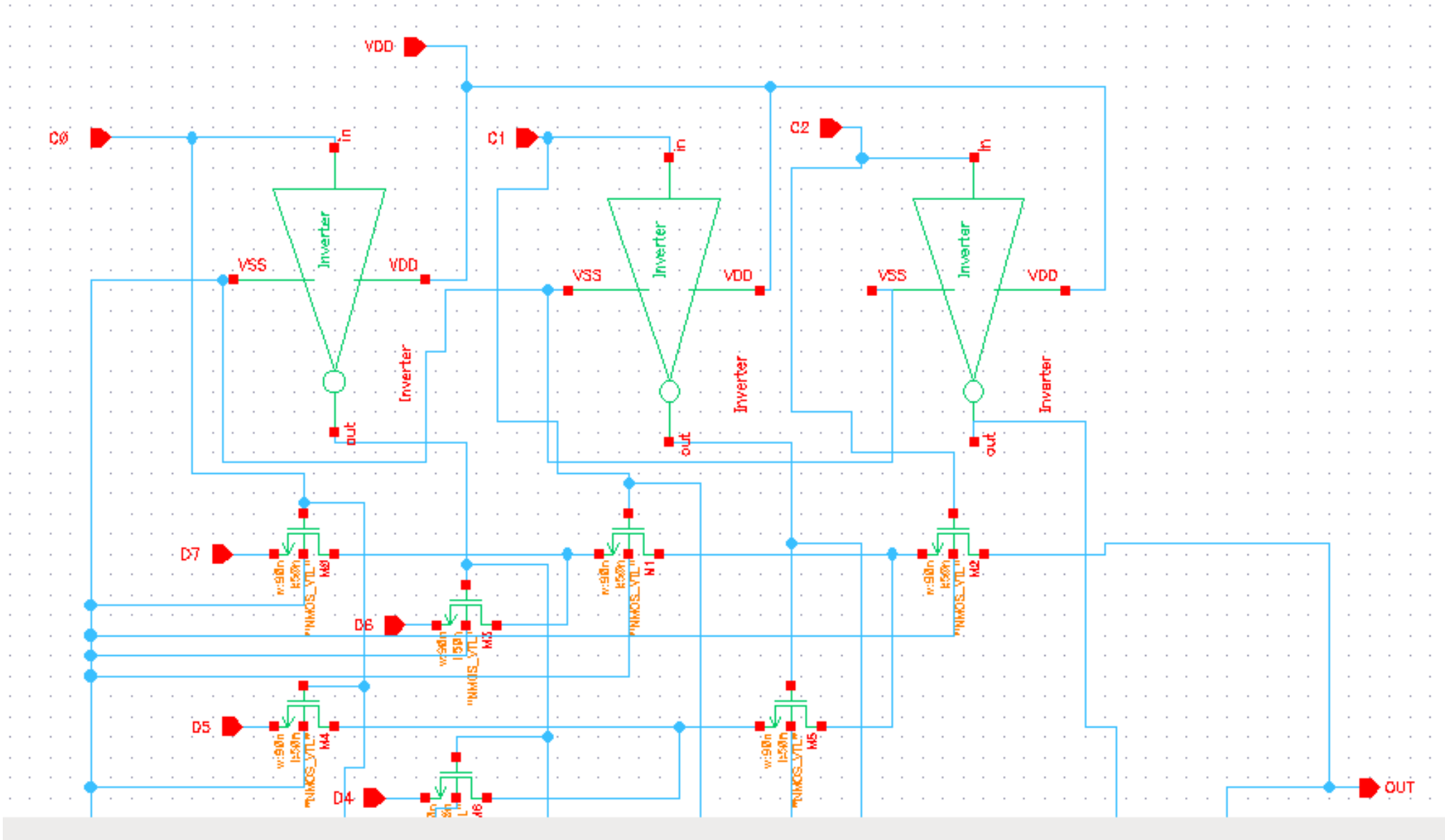

Figure 17 – 8to1 MUX Schematic (Part 1 – Top Half)

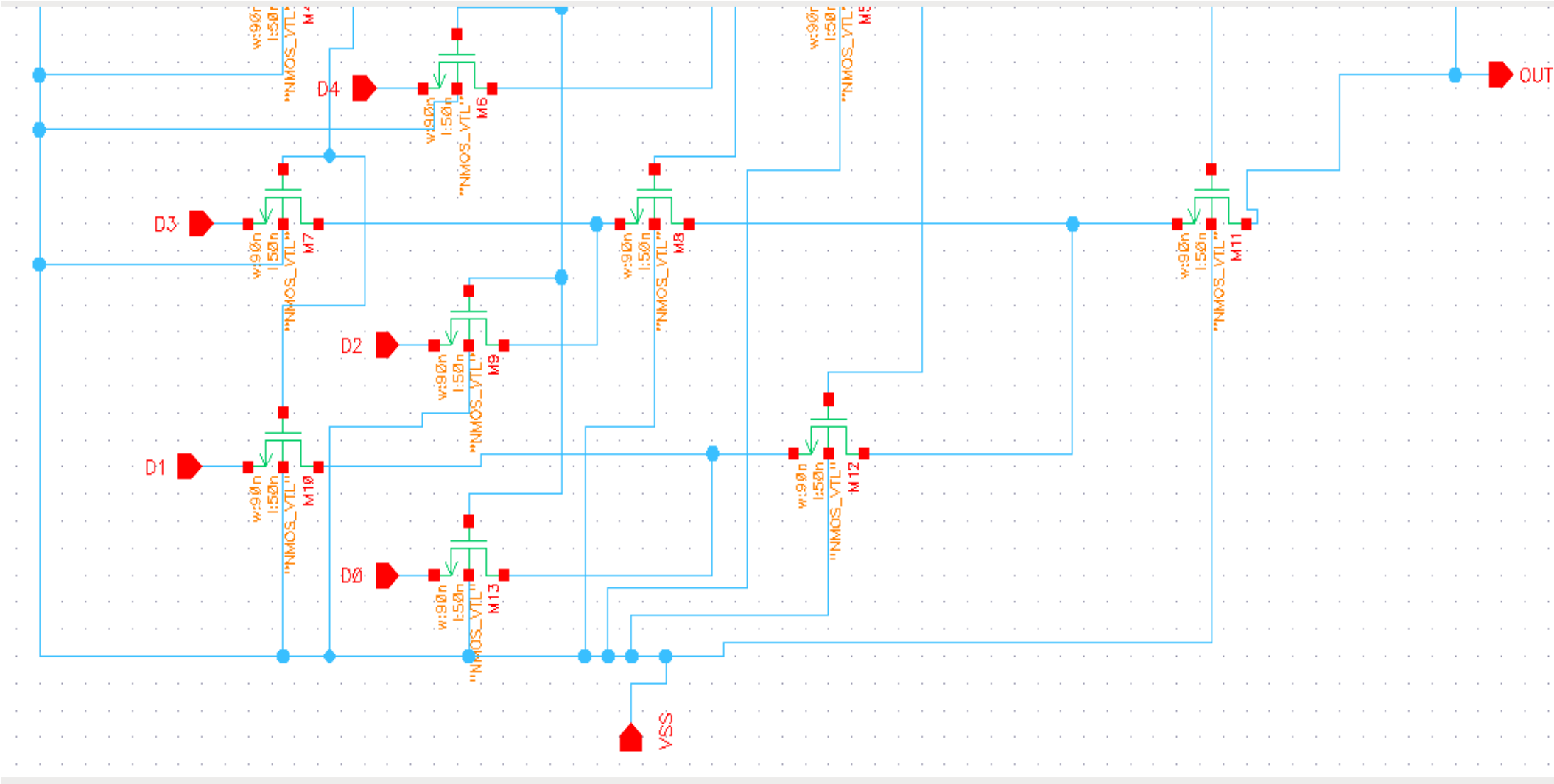

Figure 18 – 8to1 MUX Schematic (Part 2 – Bottom Half)

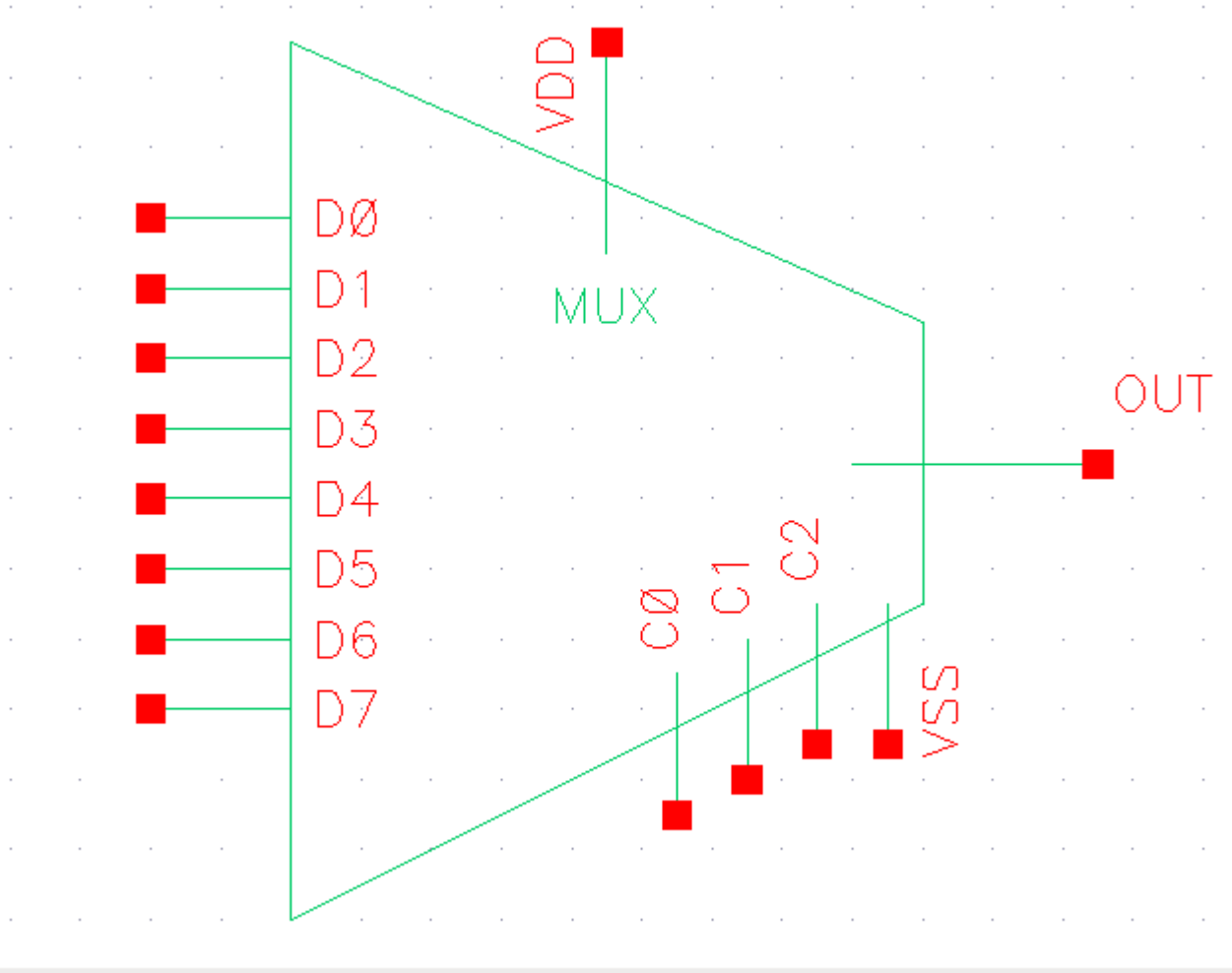

Figure 19 - 8to1 MUX Symbol

Functions of ALU (symbol called allGates)

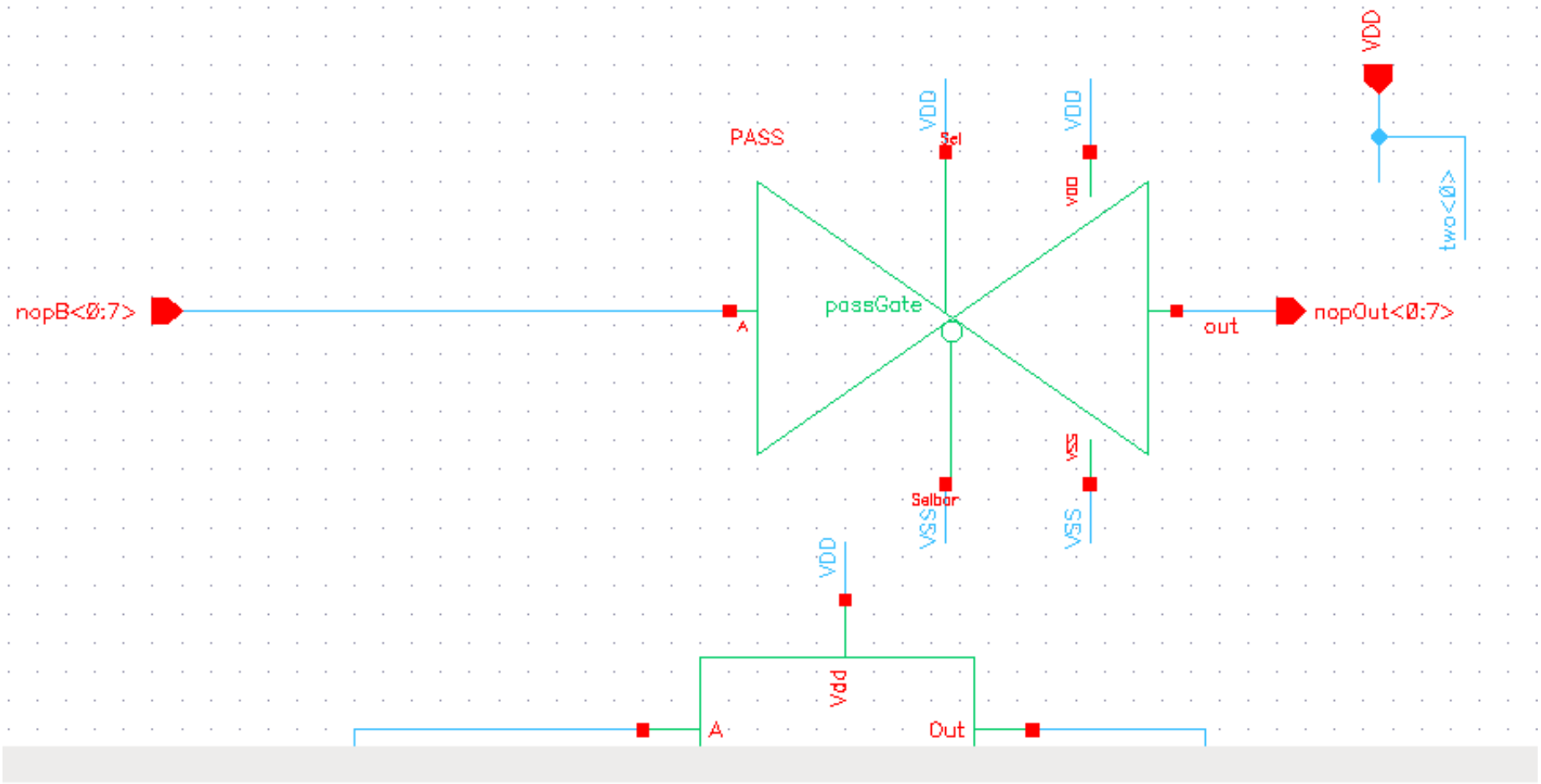

Figure 20 – allGates Schematic (Part 1)

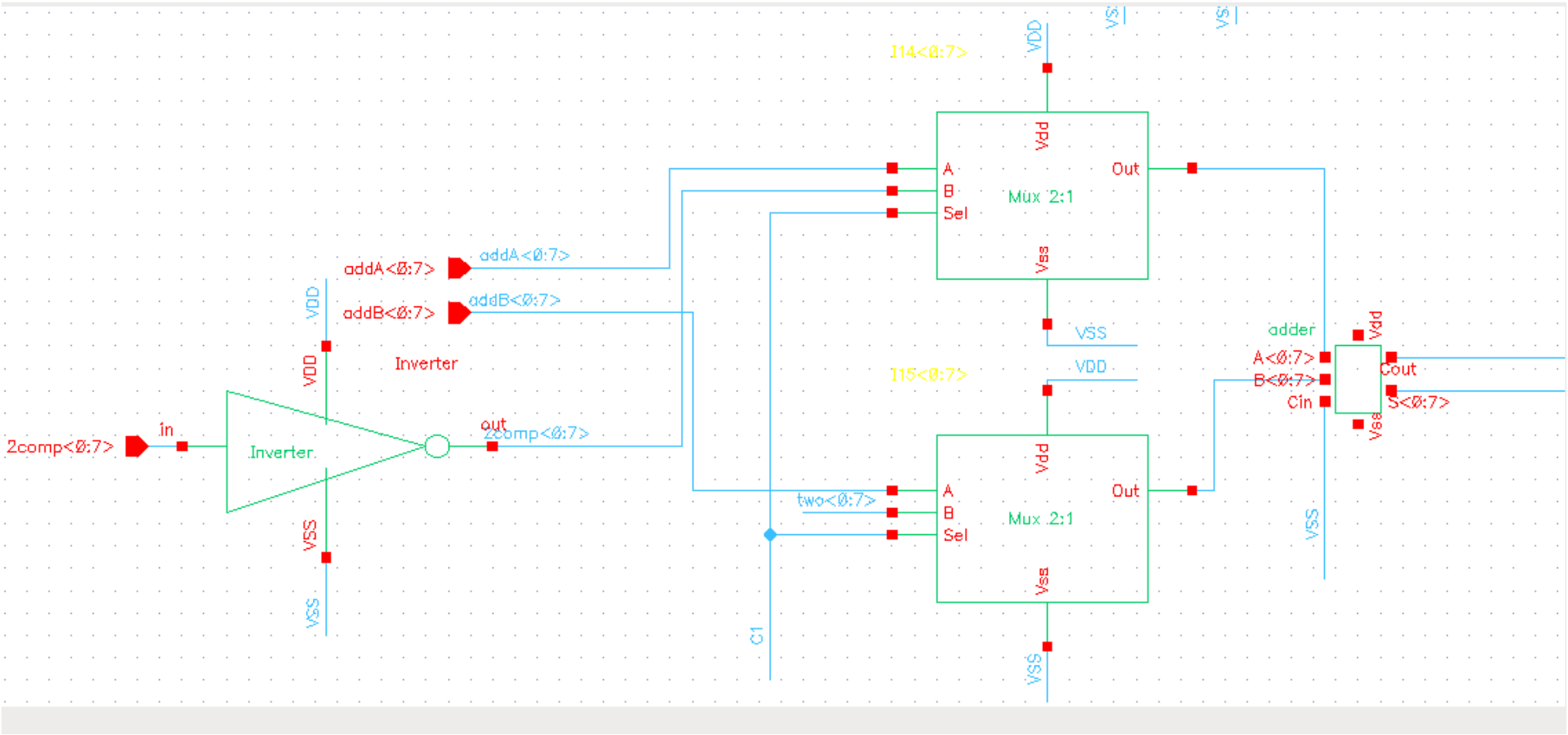

Figure 21 - allGates Schematic (Part 2)

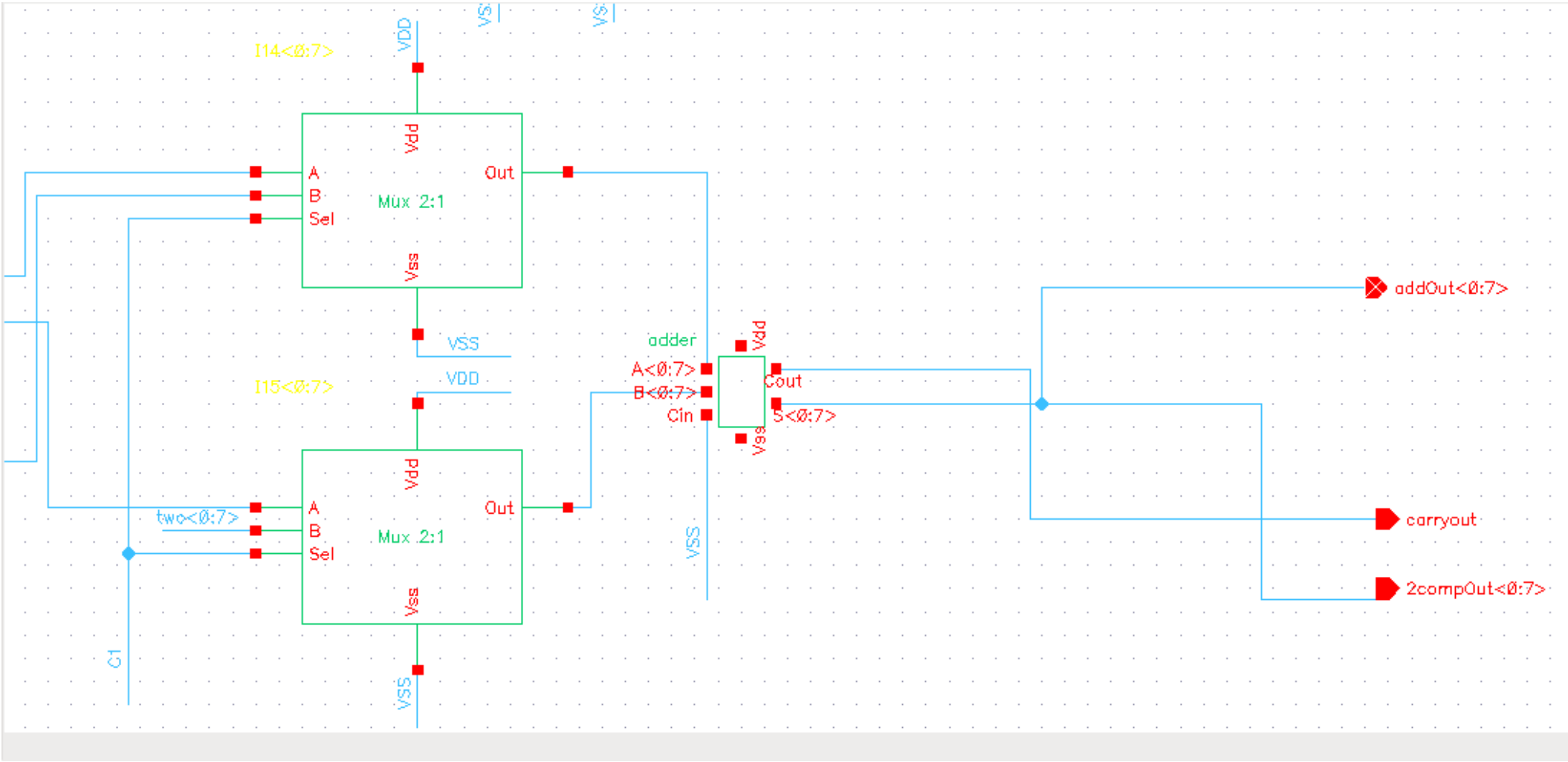

Figure 22 - allGates Schematic (Part 3)

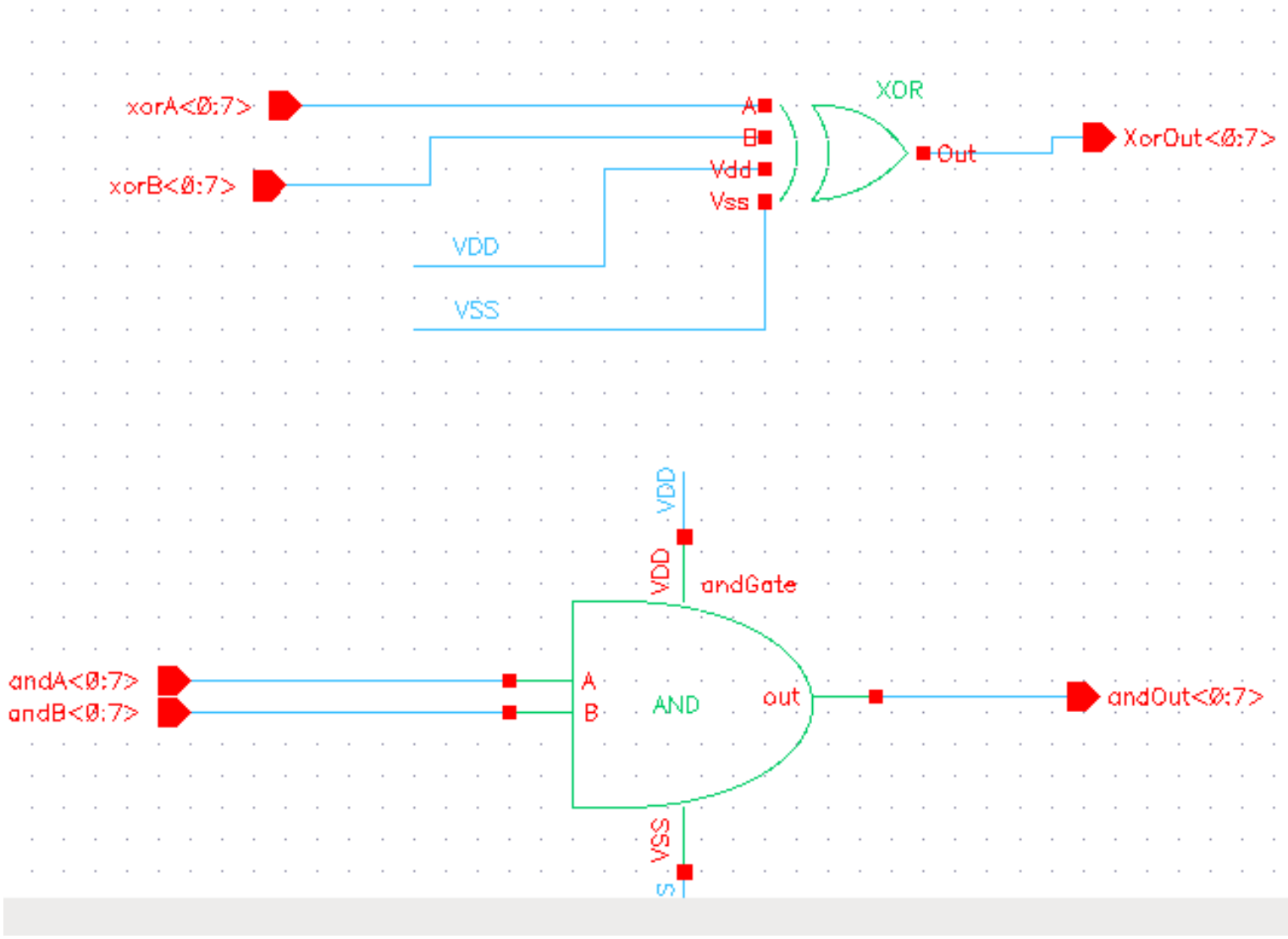

Figure 23 - allGates Schematic (Part 4)

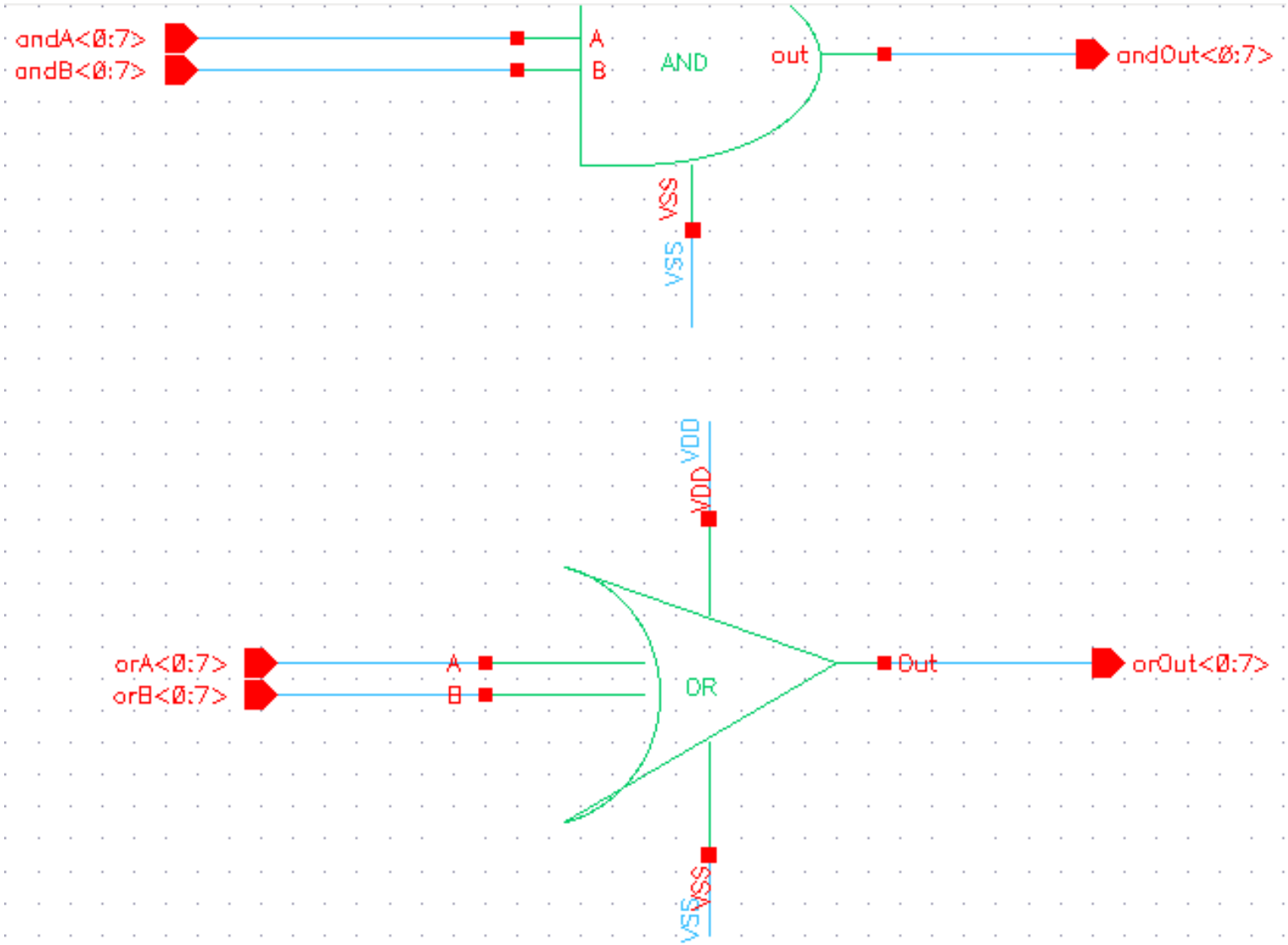

Figure 24 - allGates Schematic (Part 5)

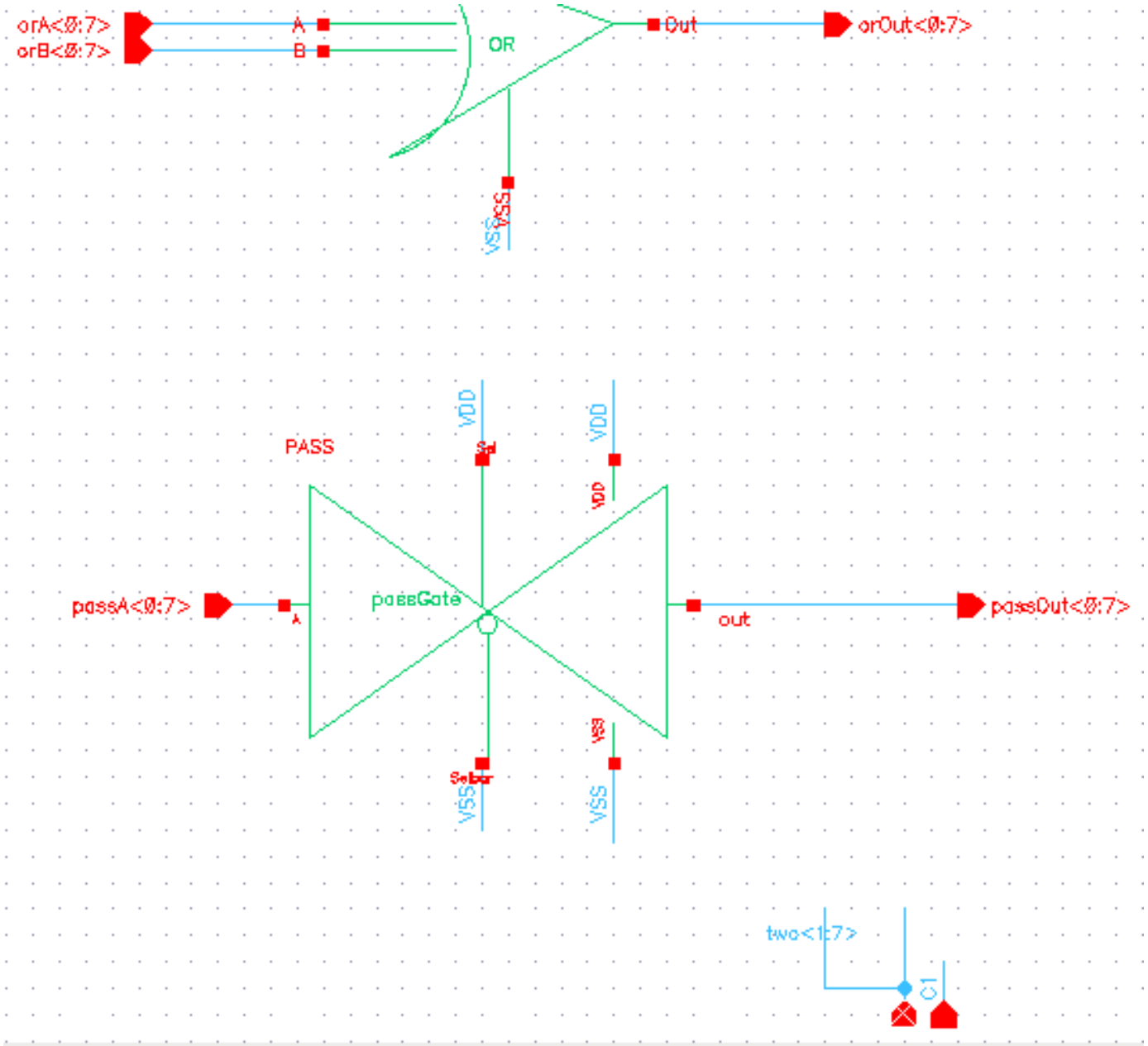

Figure 25 - allGates Schematic (Part 6)

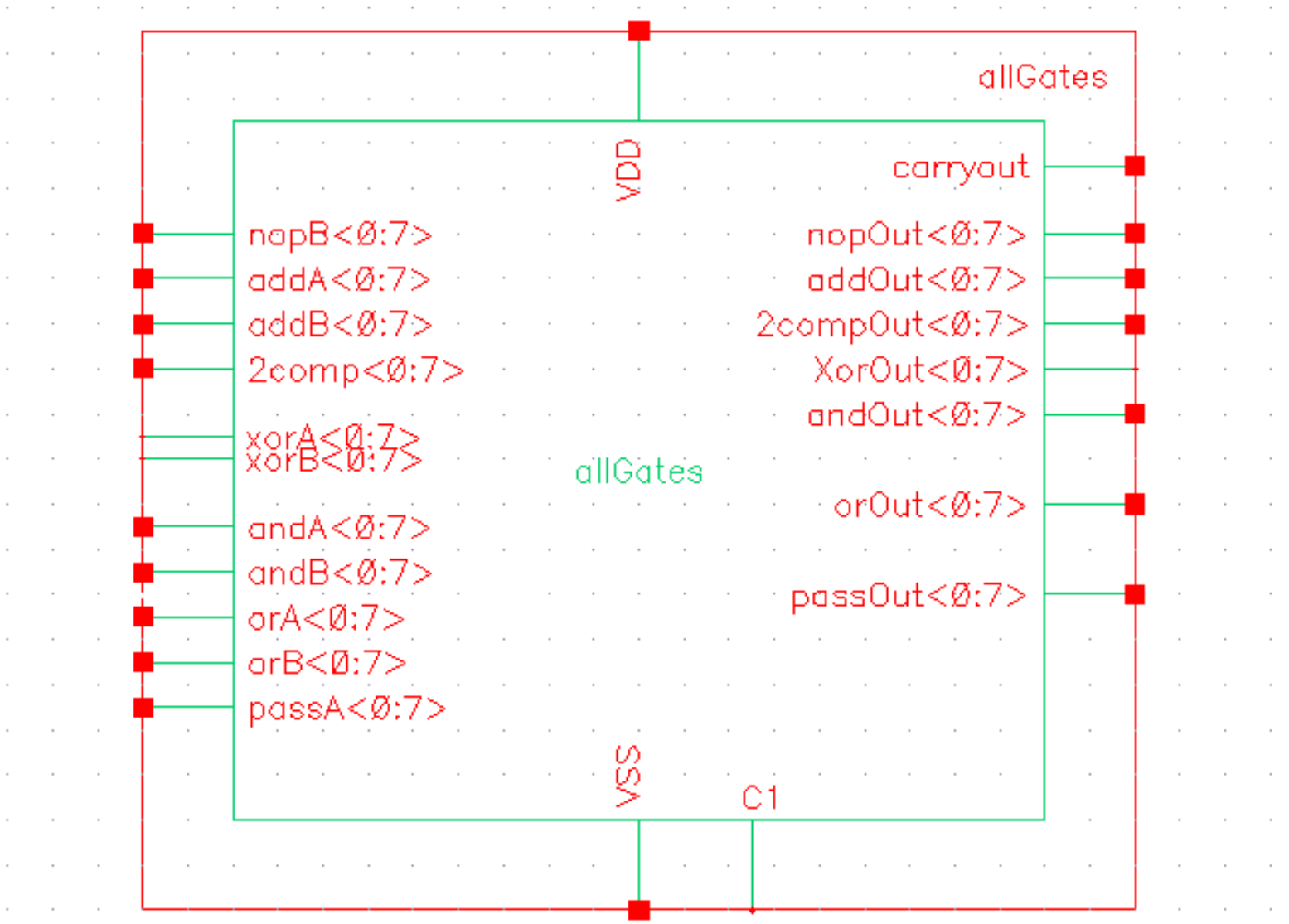

Figure 26 - allGates Symbol

ALU

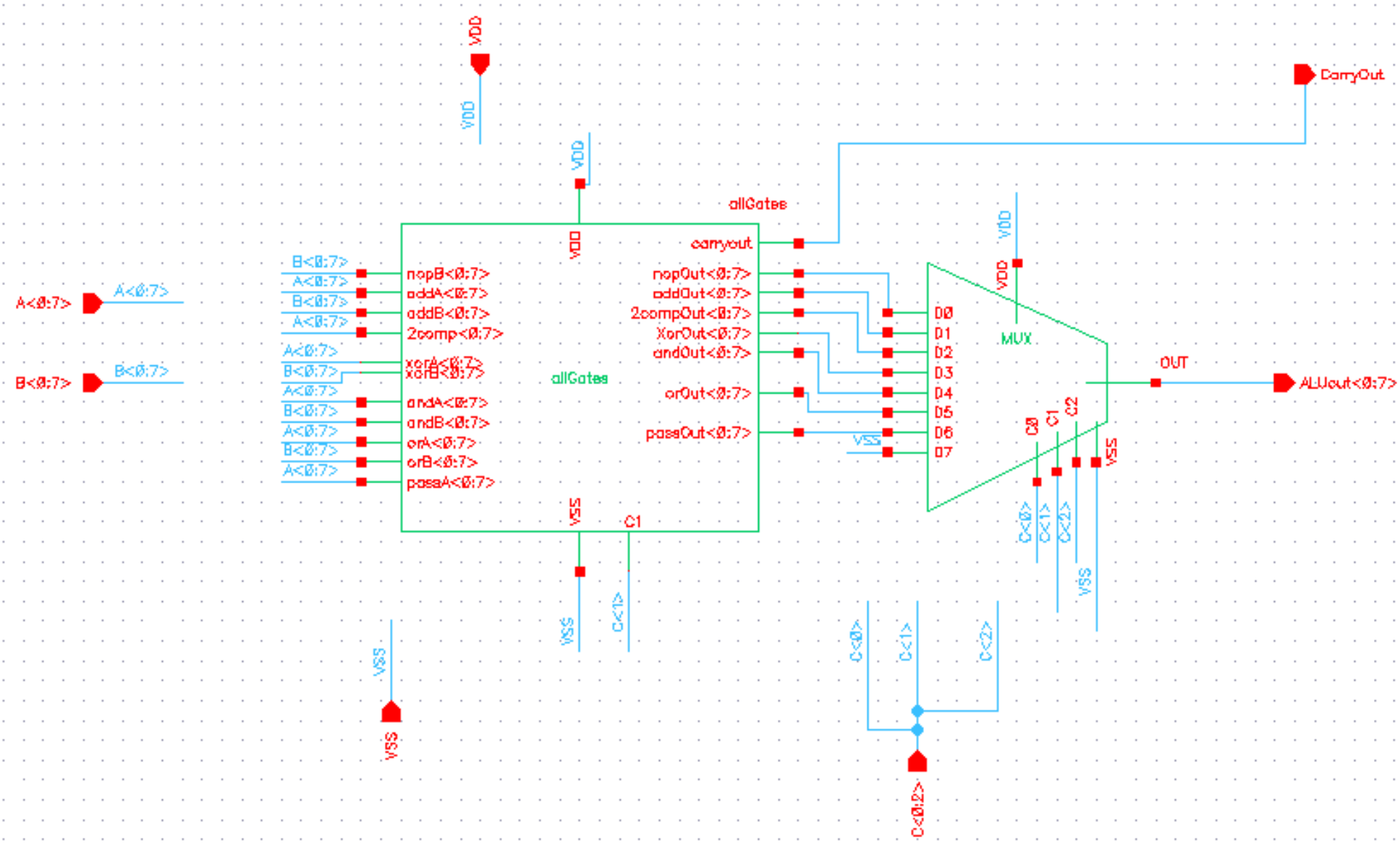

Figure 27 – ALU Schemati

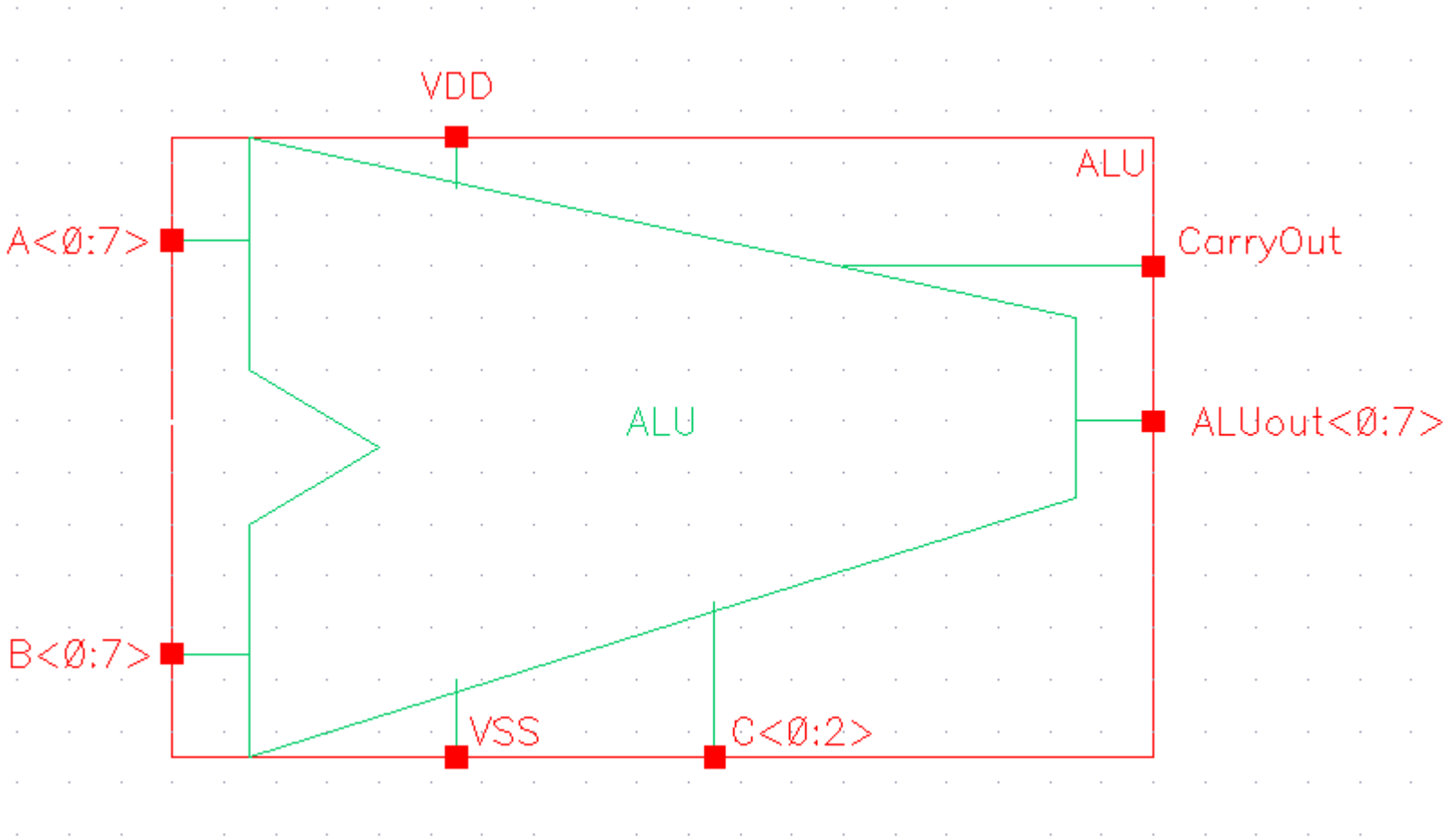

Figure 28 – ALU Symbol

Positive Edge Triggered Flip Flop

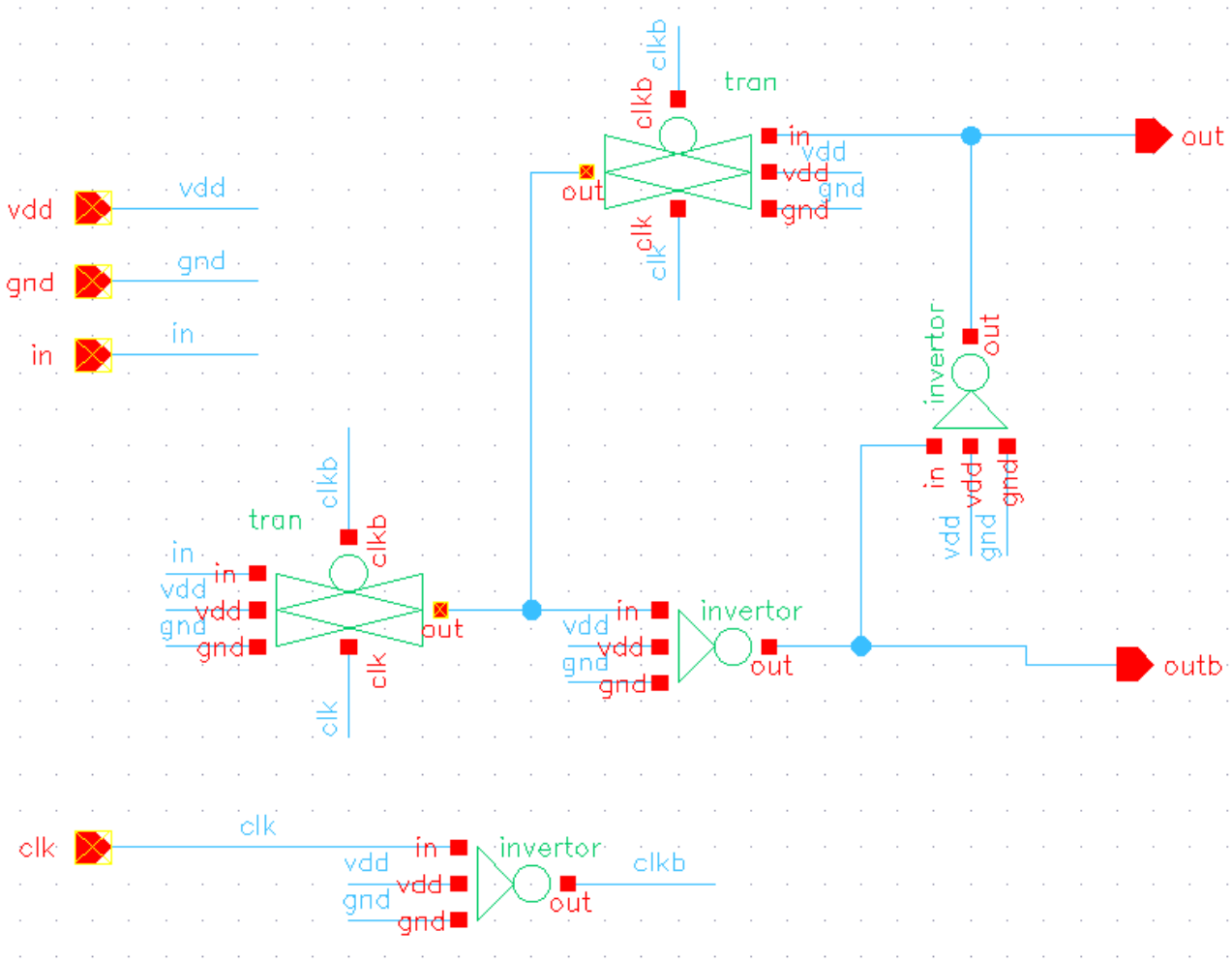

Figure 29 – Positive Edge Triggered Flip Flop Schematic

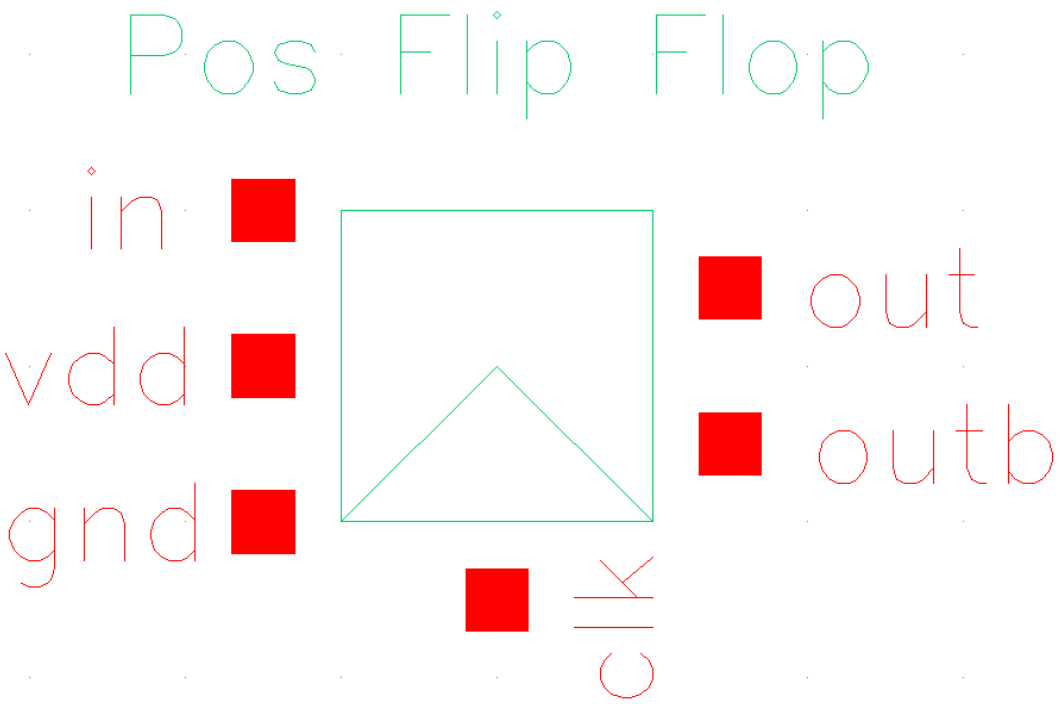

Figure 30 - Positive Edge Triggered Flip Flop Symbol

Negative Edge Triggered Flip Flop

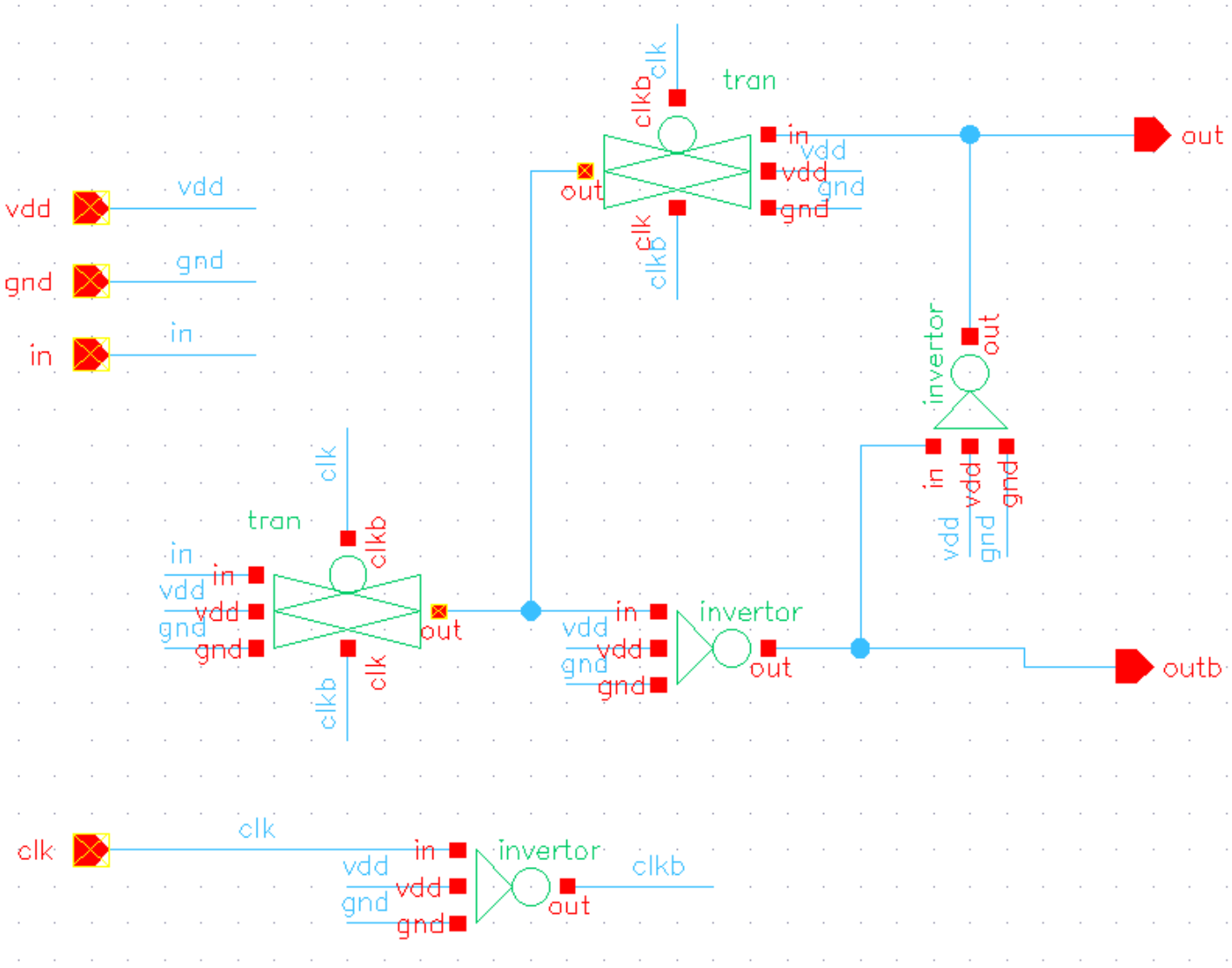

Figure 31 – Negative Edge Triggered Flip Flop Schematic

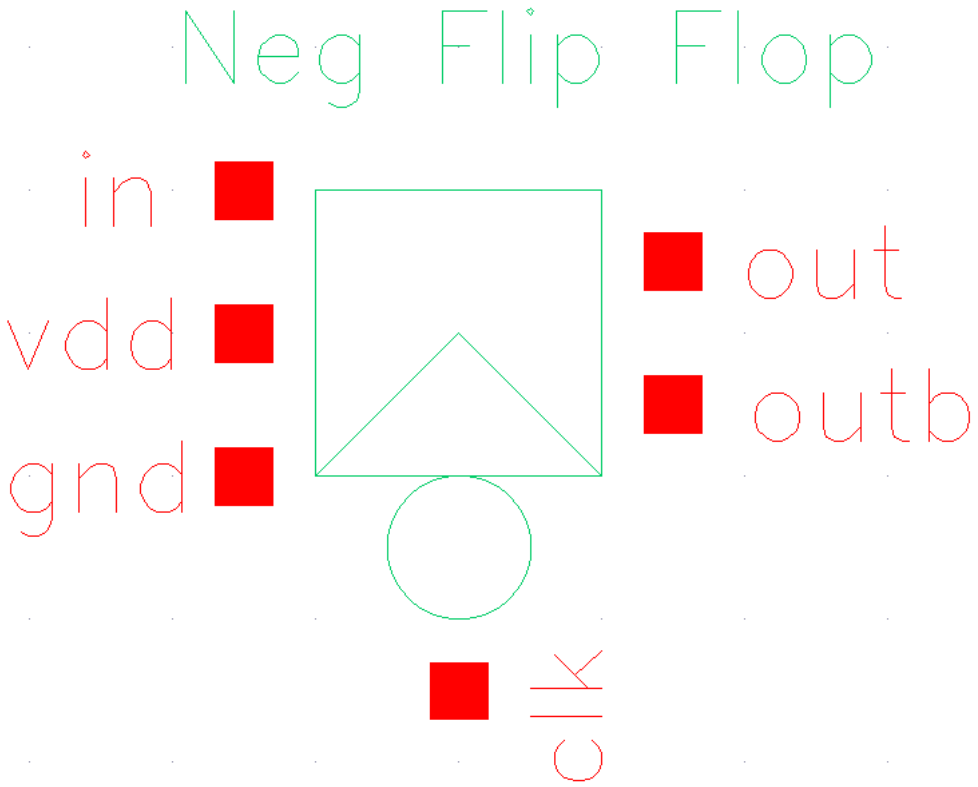

Figure 32 – Negative Edge Triggered Flip Flop Symbol

Register

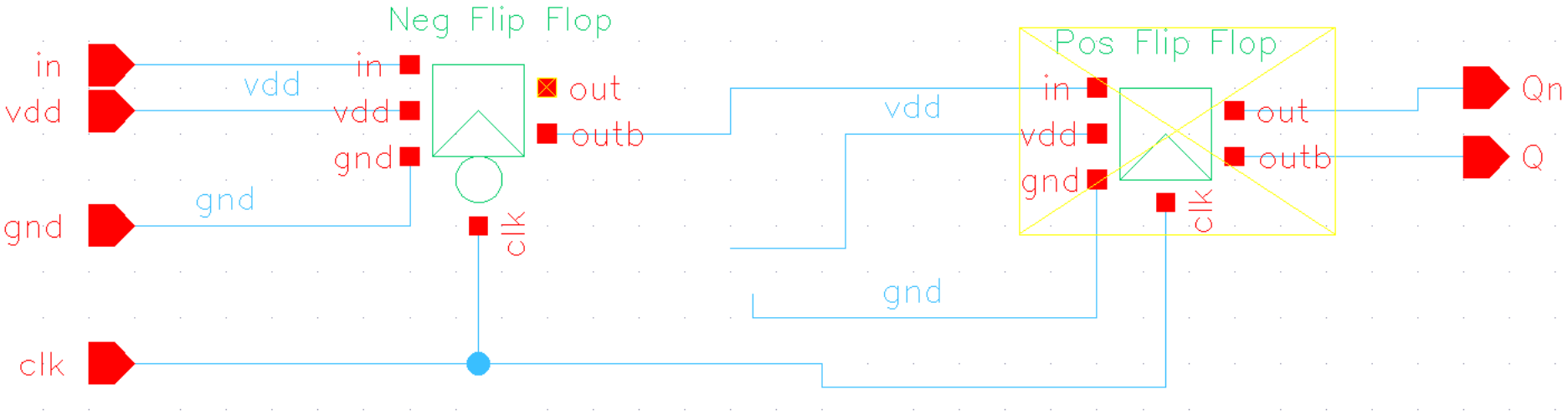

Figure 33 – Register/D-Flip Flop Schematic

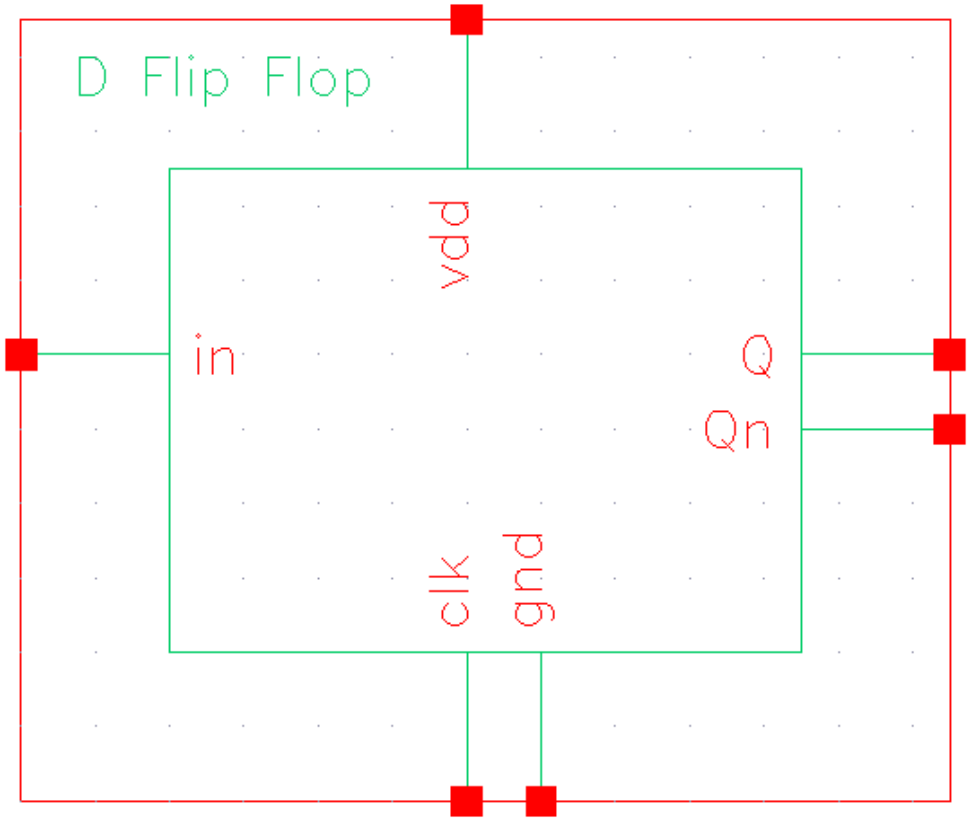

Figure 34 – Register/D-Flip Flop Symbol

FINAL DESIGN

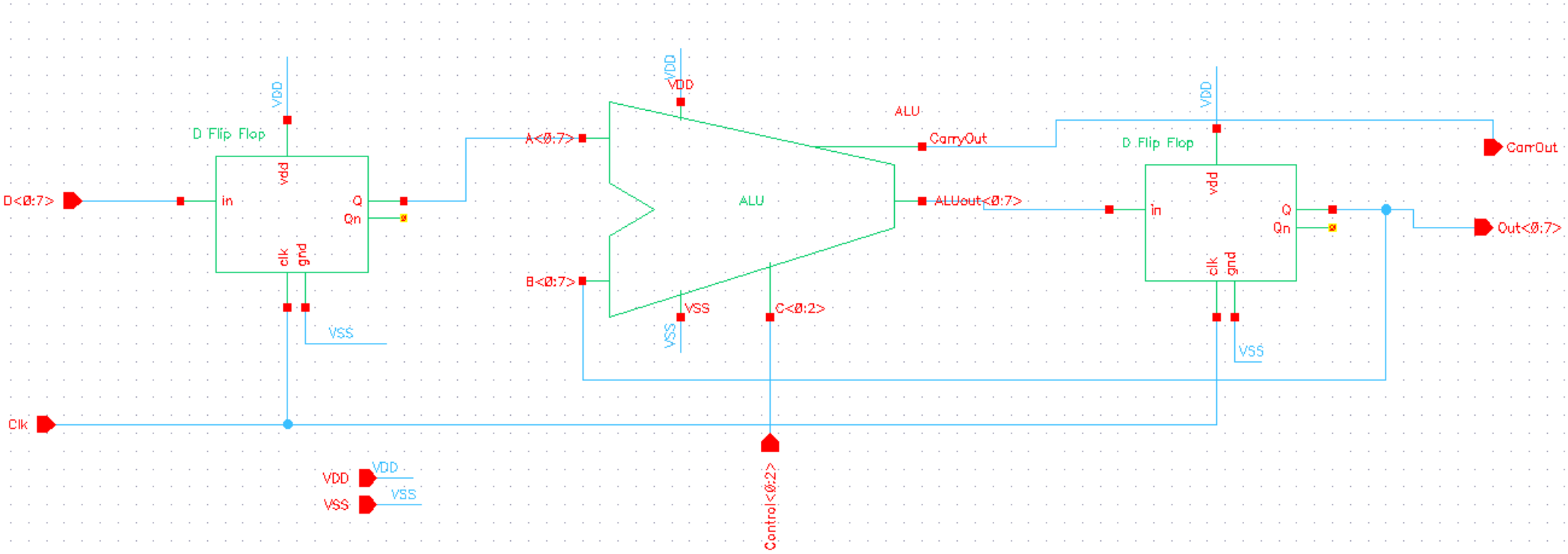

Figure 35 – Final Design Schematic

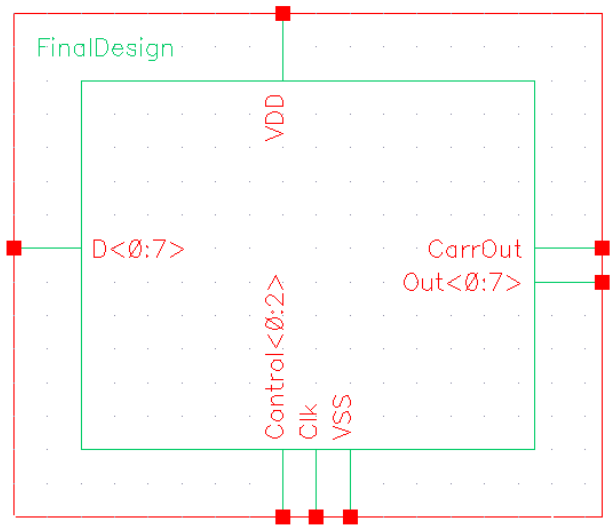

Figure 36 – Final Design Symbol

Simulation Plots

AND – The first figure is without the two inverters after the inputs and the second figure is with the two inverters. We concluded that they are about the same

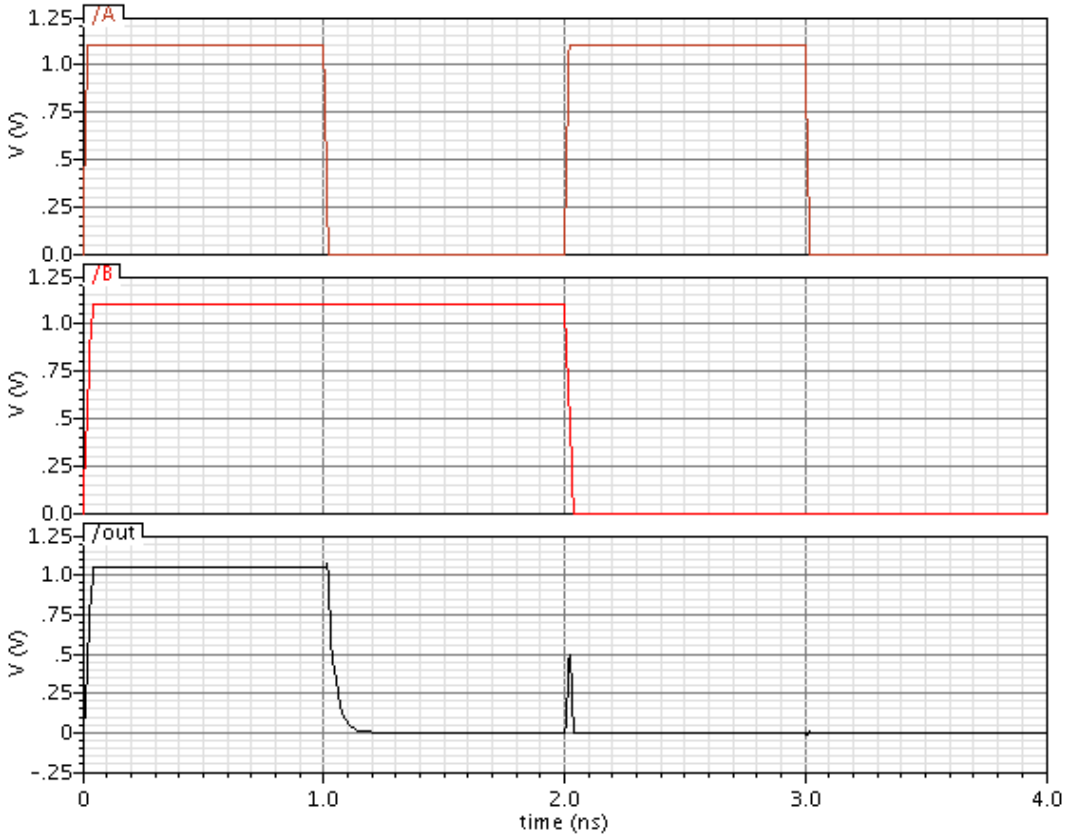

Figure 37 –AND Simulation

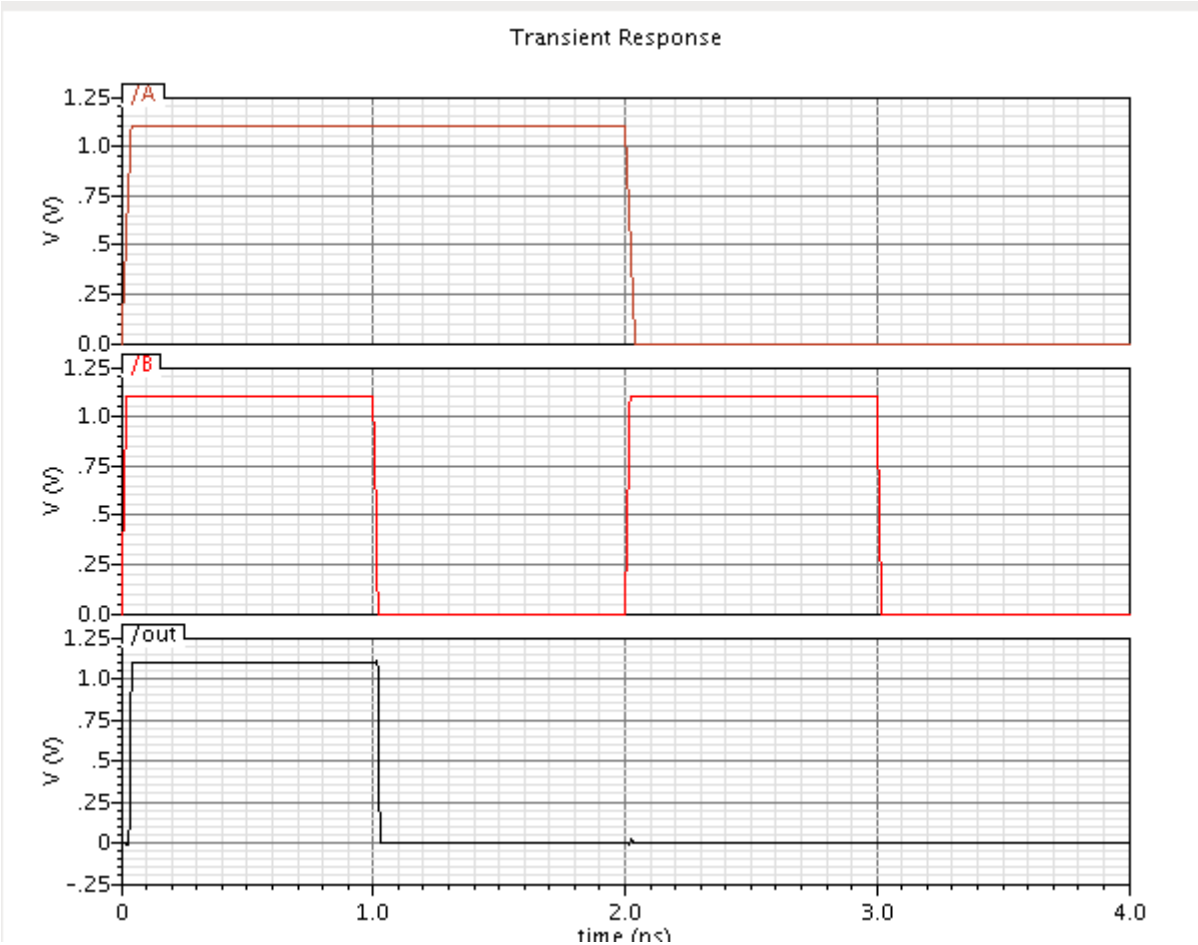

Figure 38 – AND Simulation w/ 2 Inverters at Inputs

2bitADDER

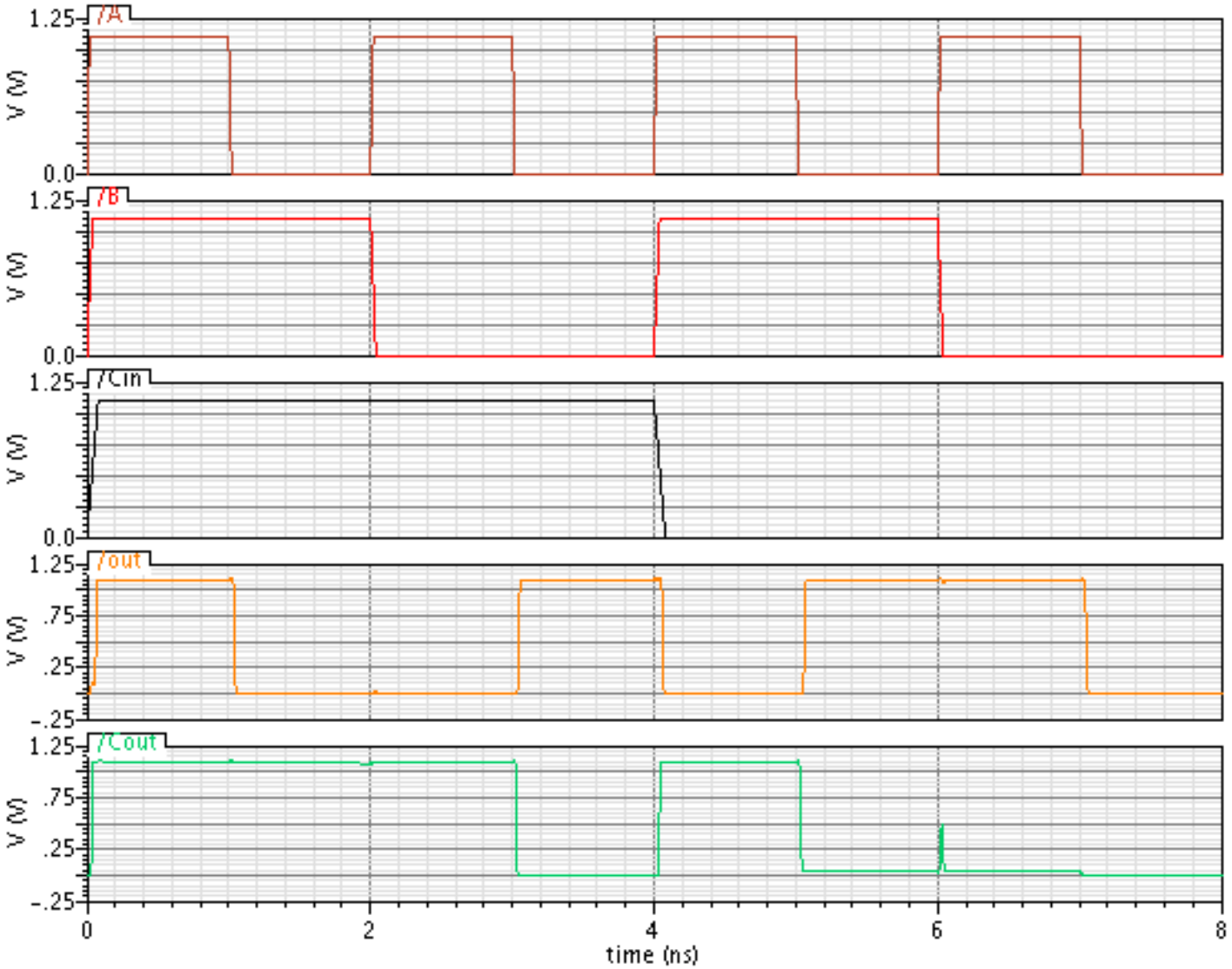

Figure 39 – Adder Simulation

XOR

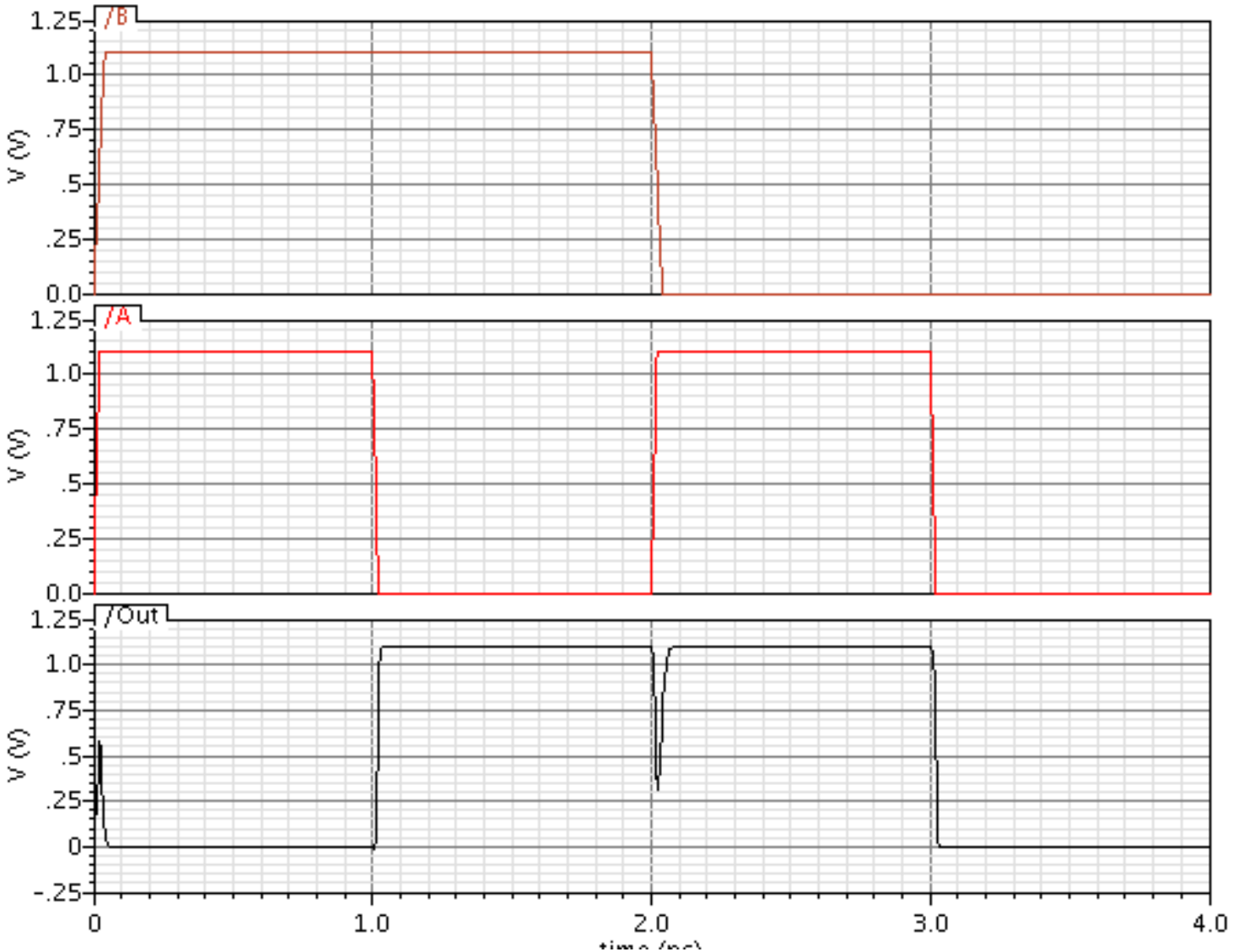

Figure 40 – XOR Simulatin

OR

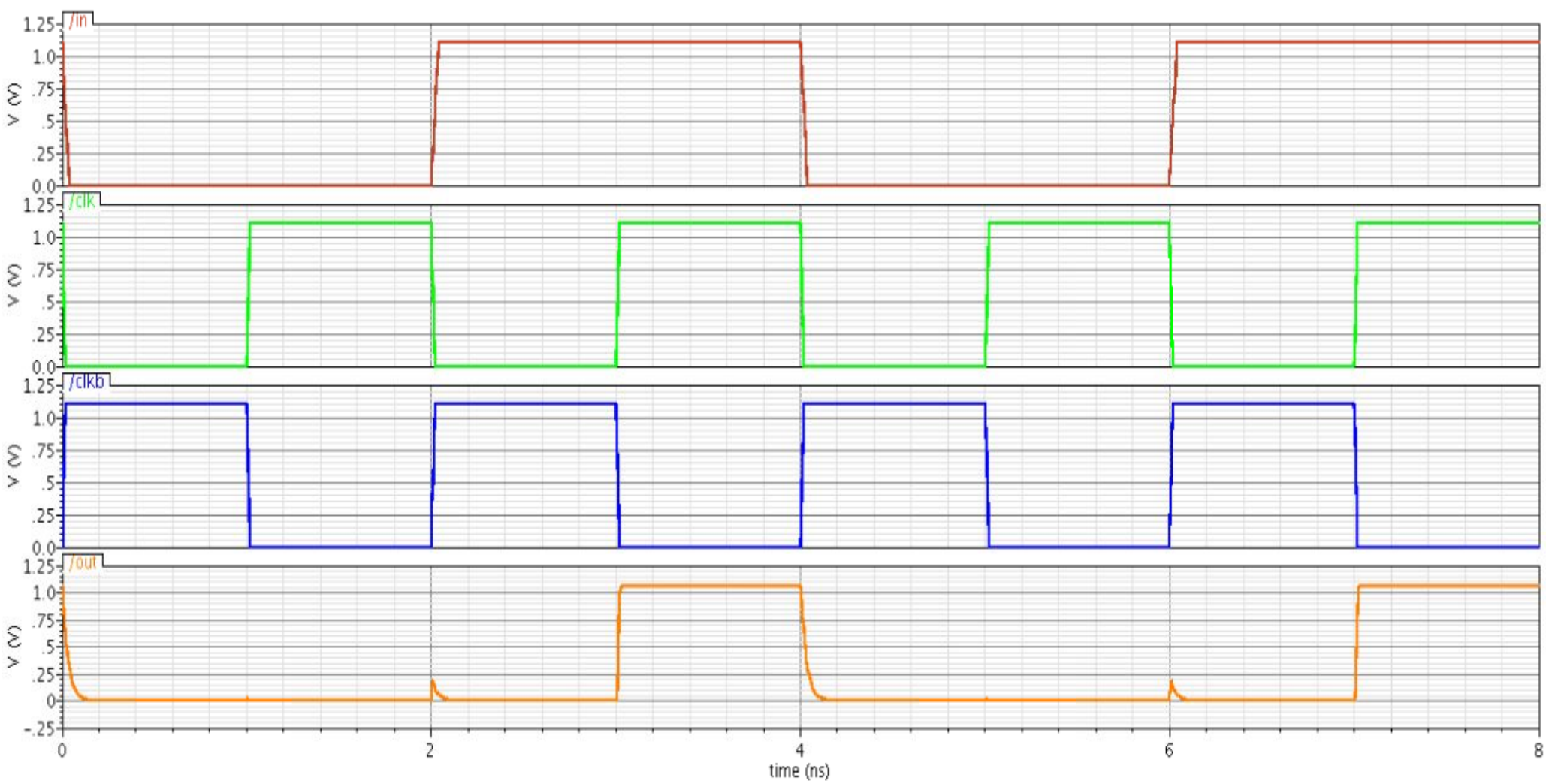

Figure 41 – OR Simulation

8to1 MUX – The first three figures show the propagation of D0 through the MUX with control bits 000 (c2c1c0) and all other inputs D1-D7 (first 2 figures) but for the rest of the figures these are omitted for space

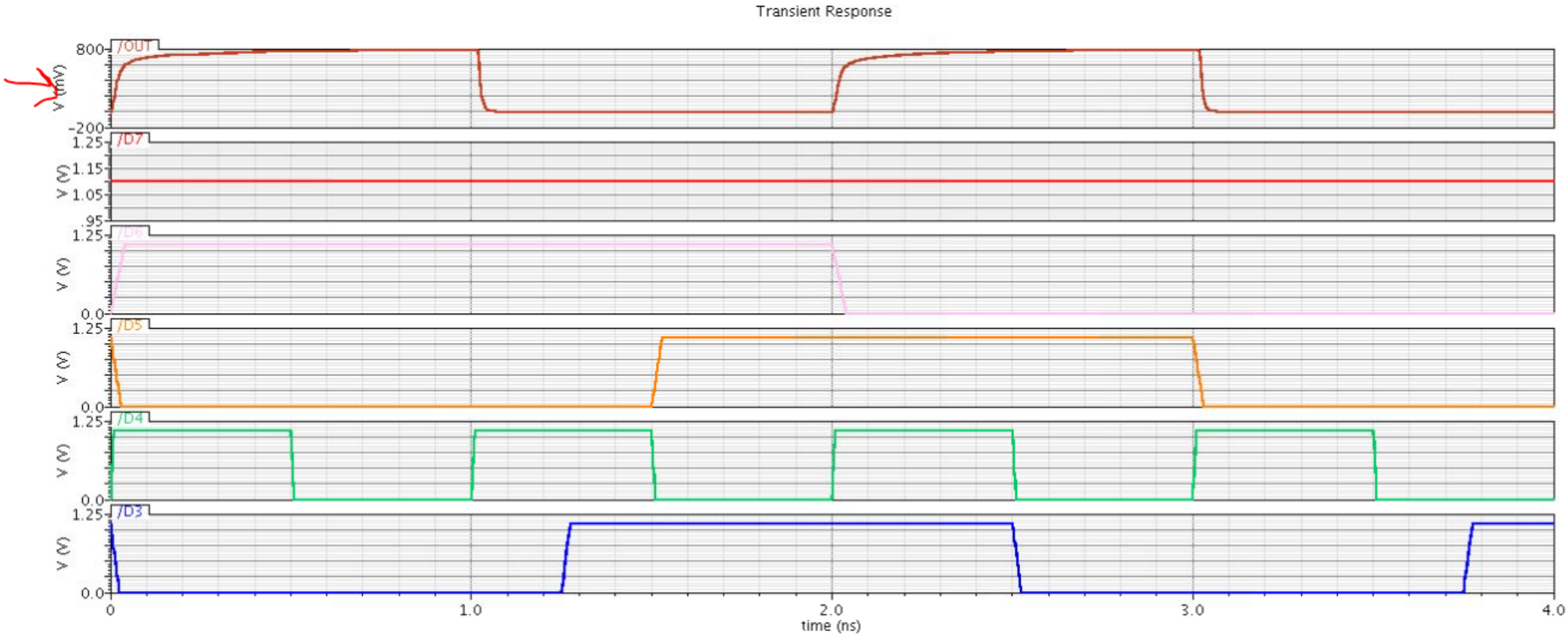

Figure 42 – 8to1 MUX Simulation w/ all inputs plotted (here: D3-D7); output is D0 Propagated

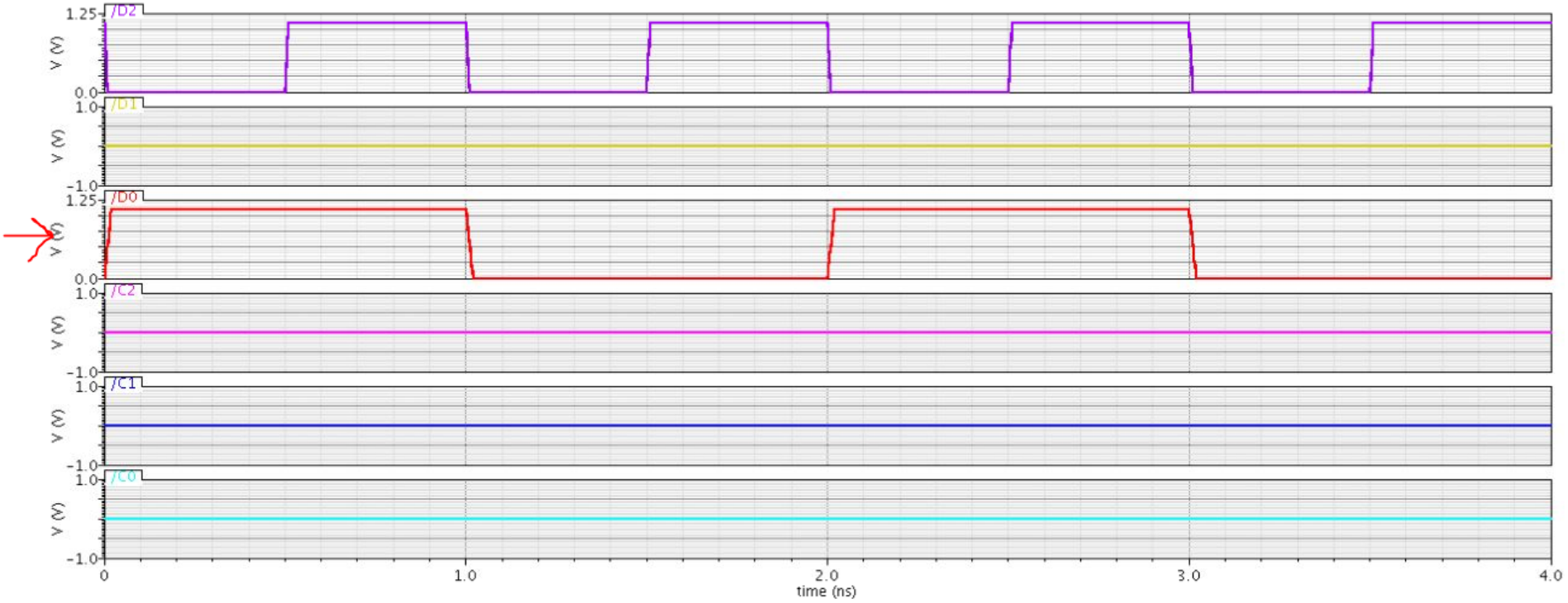

Figure 43 – 8to1 MUX Simulation w/ all inputs plotted (here: C0-C2 and D0-D2); D0 propagates to output

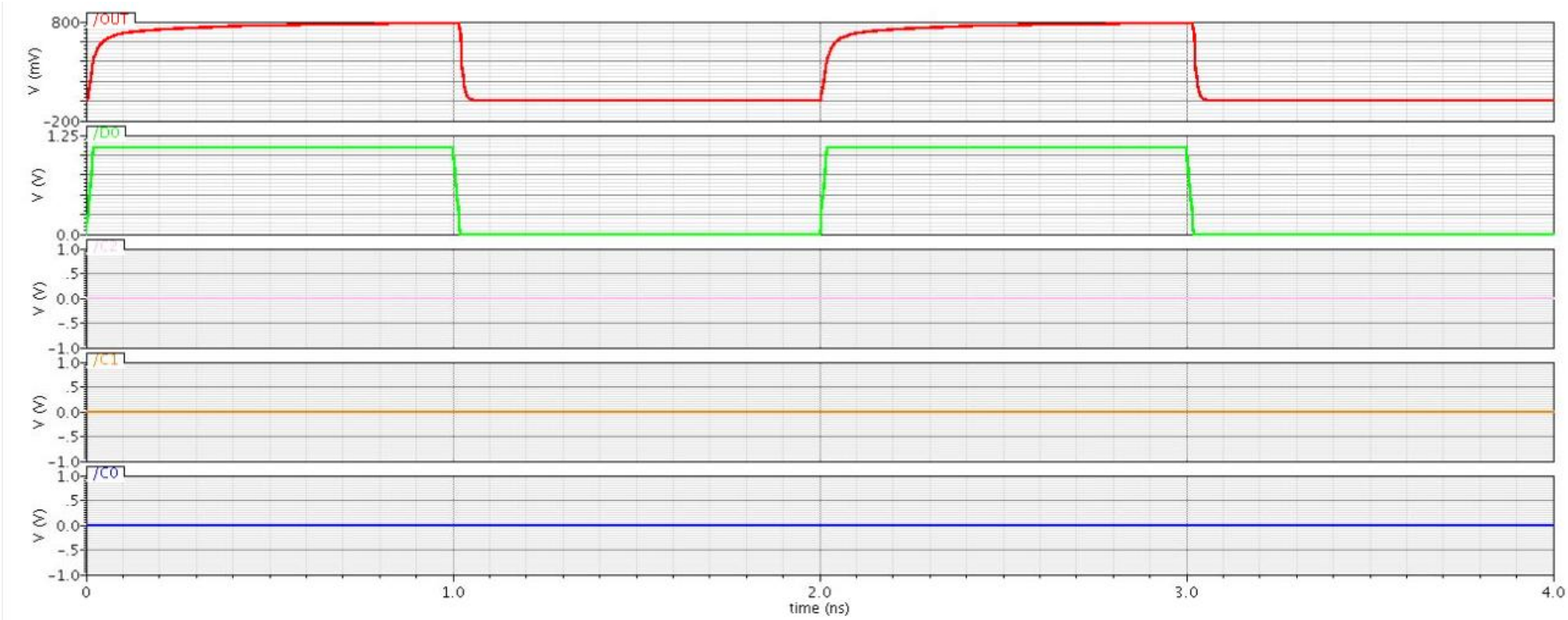

Figure 44 – 8to1 MUX Simulation w/ D0 propagating

Propagation of D1 w/ control 001

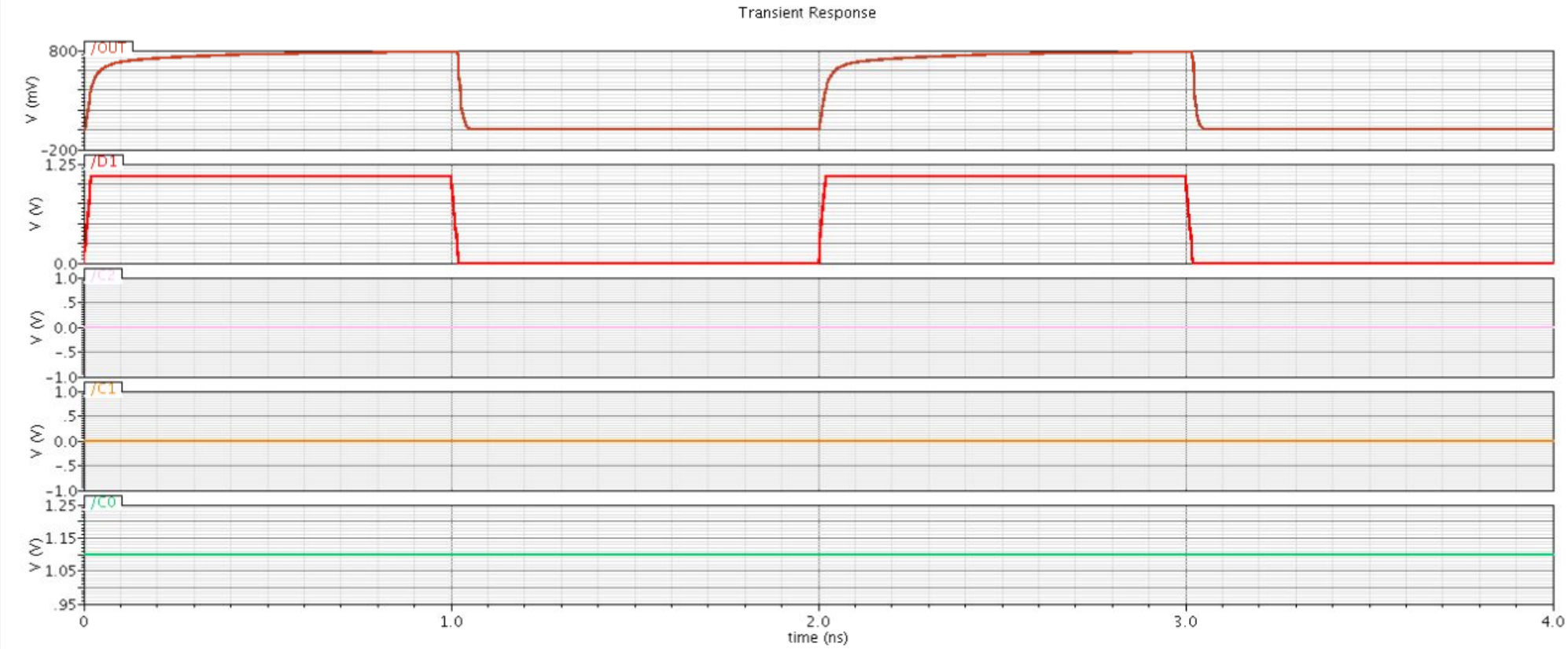

Figure 45 – 8to1 MUX Simulation w/ D1 propagating

Propagation of D2 w/ control 010

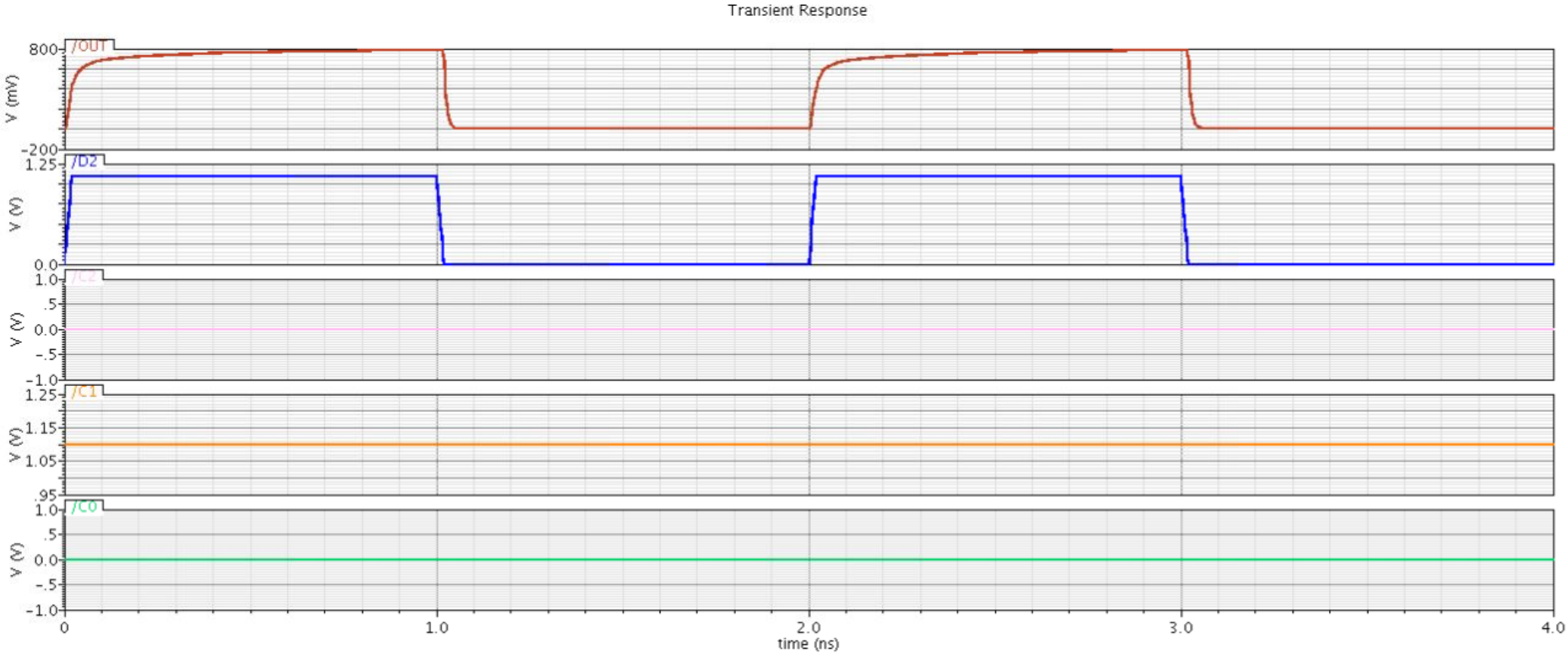

Figure 46 – 8to1 MUX Simulation w/ D2 propagating

Propagation of D3 w/ control 011

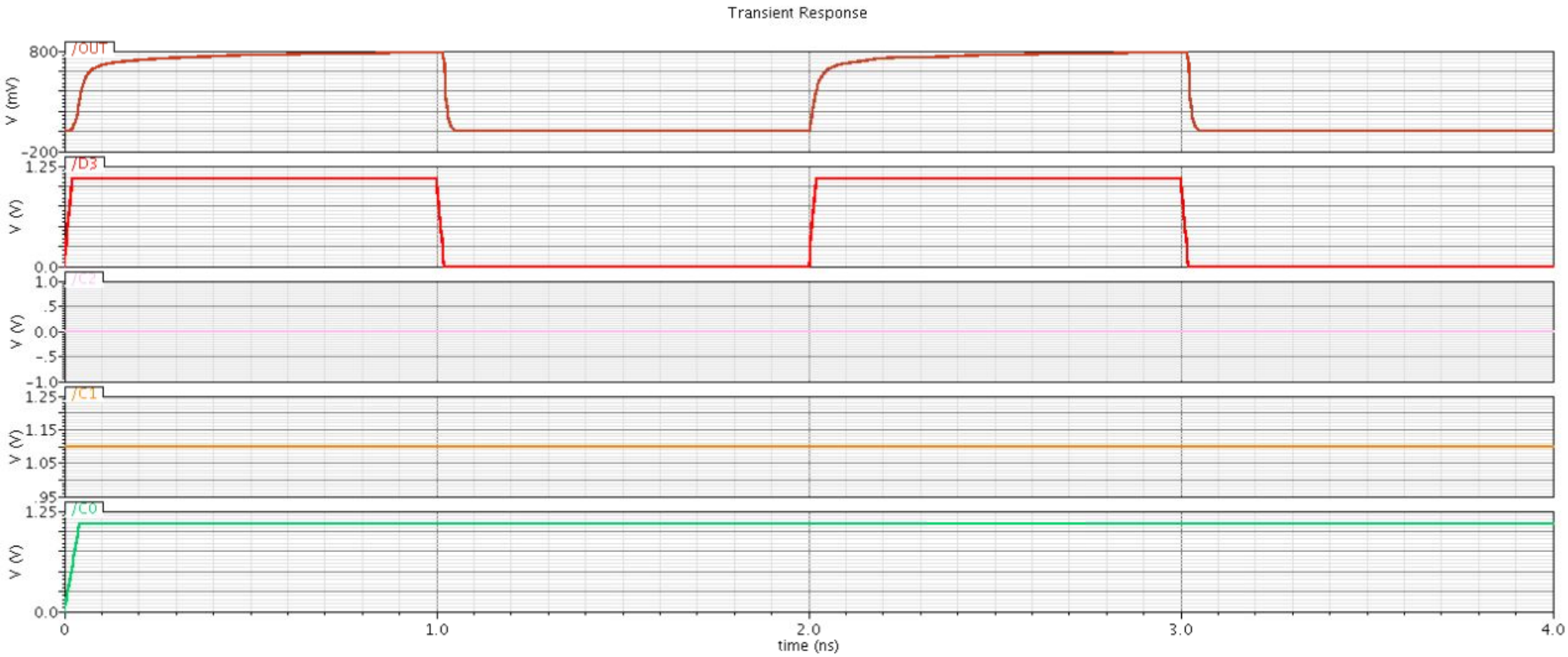

Figure 47 – 8to1 MUX Simulation w/ D3 propagating

Propagation of D4 w/ control 100

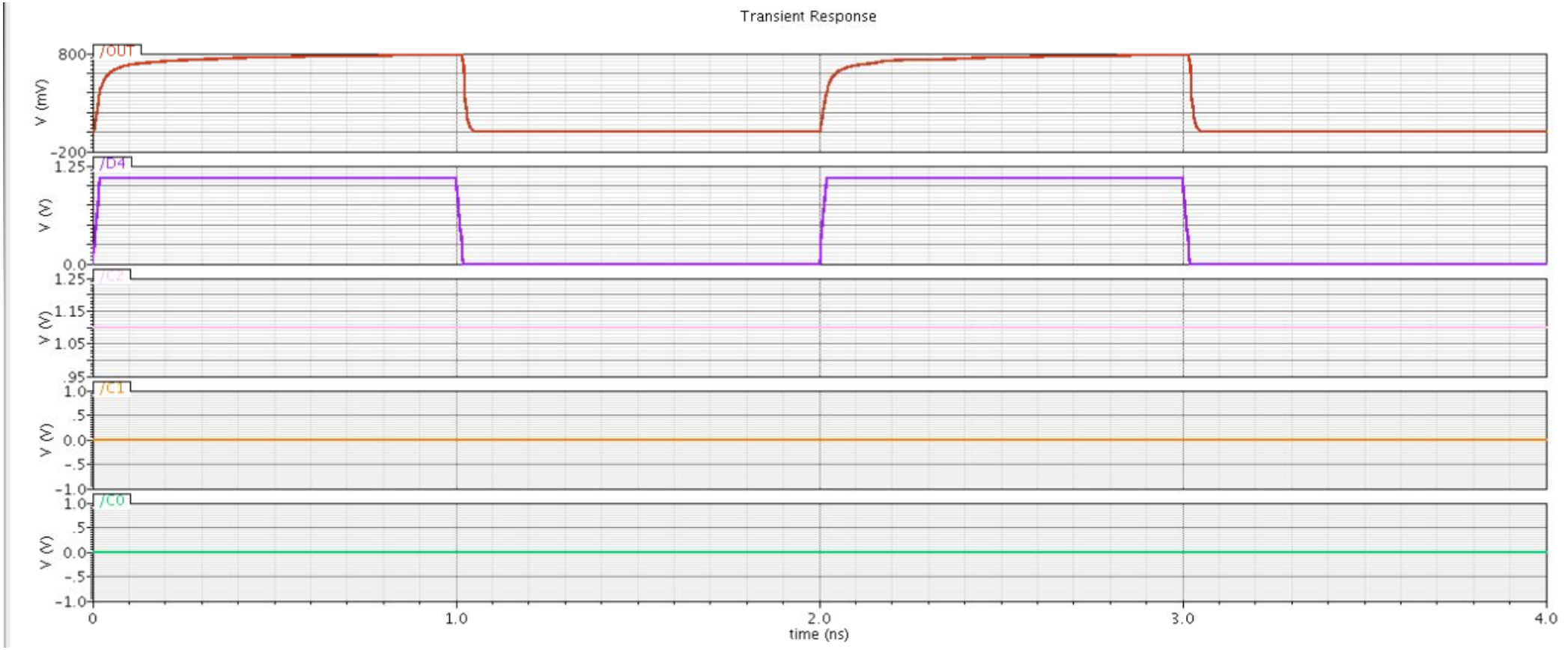

Figure 48 – 8to1 MUX Simulation w/ D4 propagating

Propagation of D5 w/ control 101

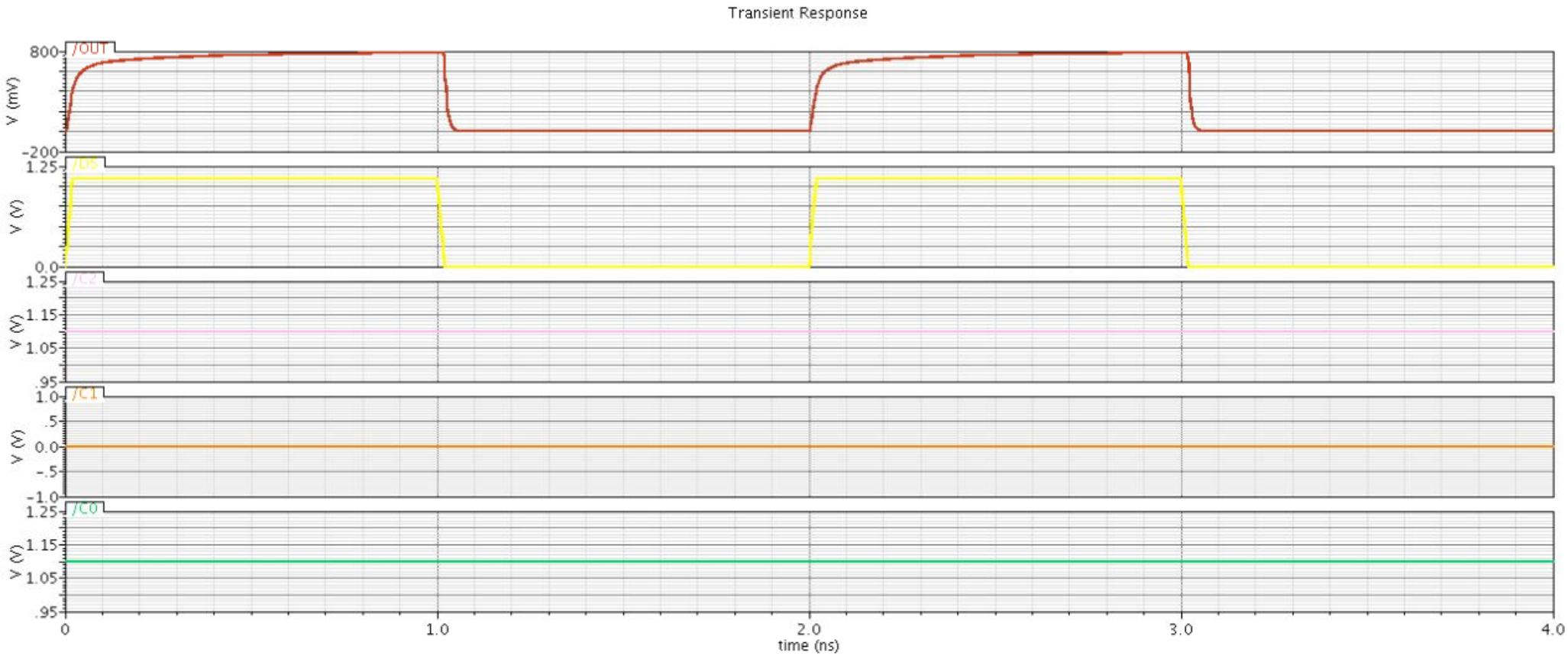

Figure 49 – 8to1 MUX Simulation w/ D5 propagating

Propagation of D6 w/ control 110

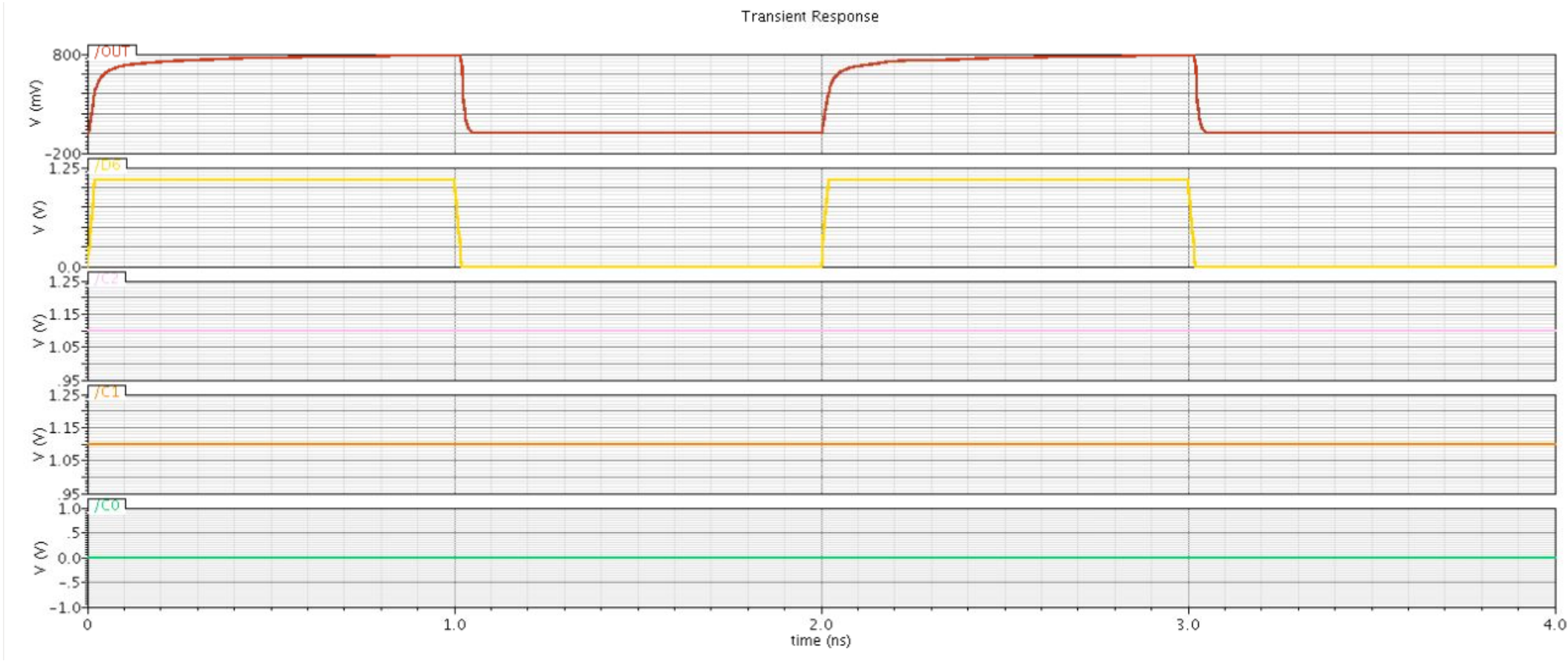

Figure 50 – 8to1 MUX Simulation w/ D6 propagating

Propagation of D7 w/ control 111

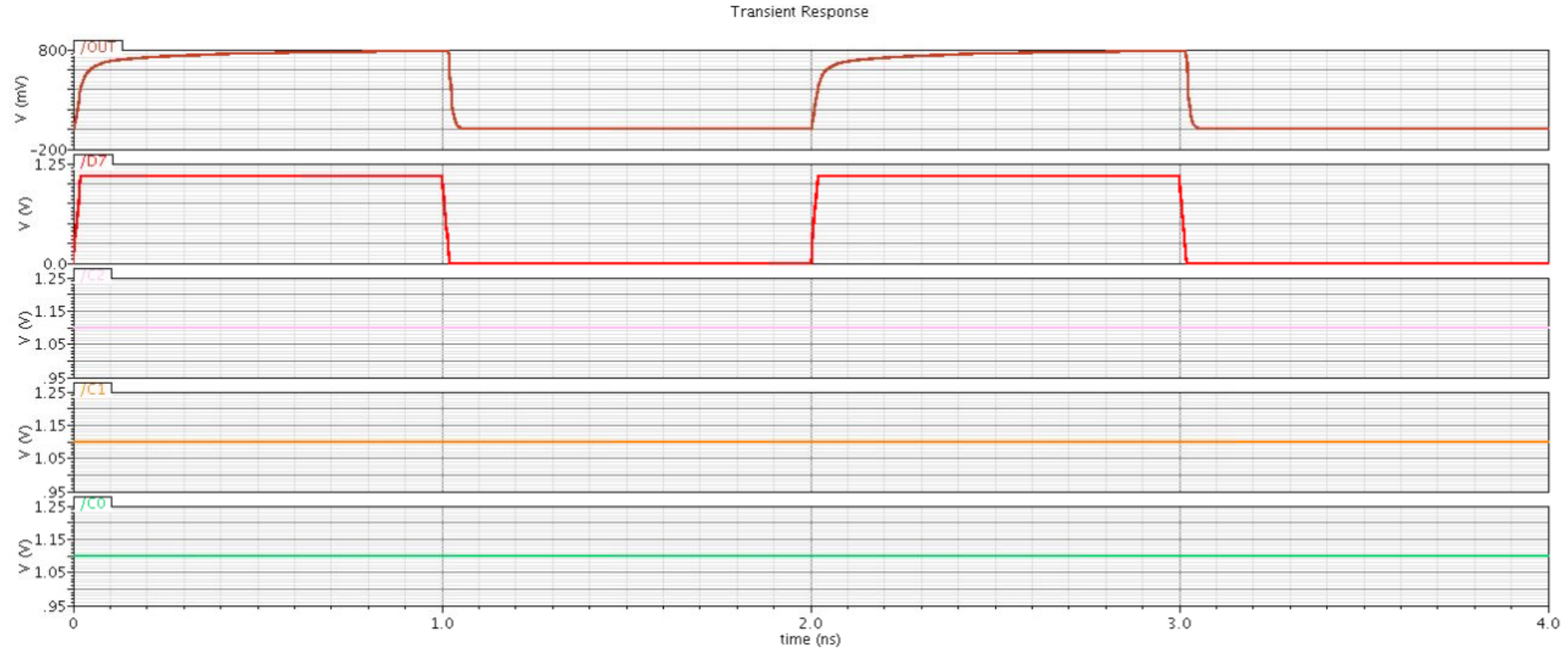

Figure 51 – 8to1 MUX Simulation w/ D7 propagating

Positive Edge Triggered Flip Flop

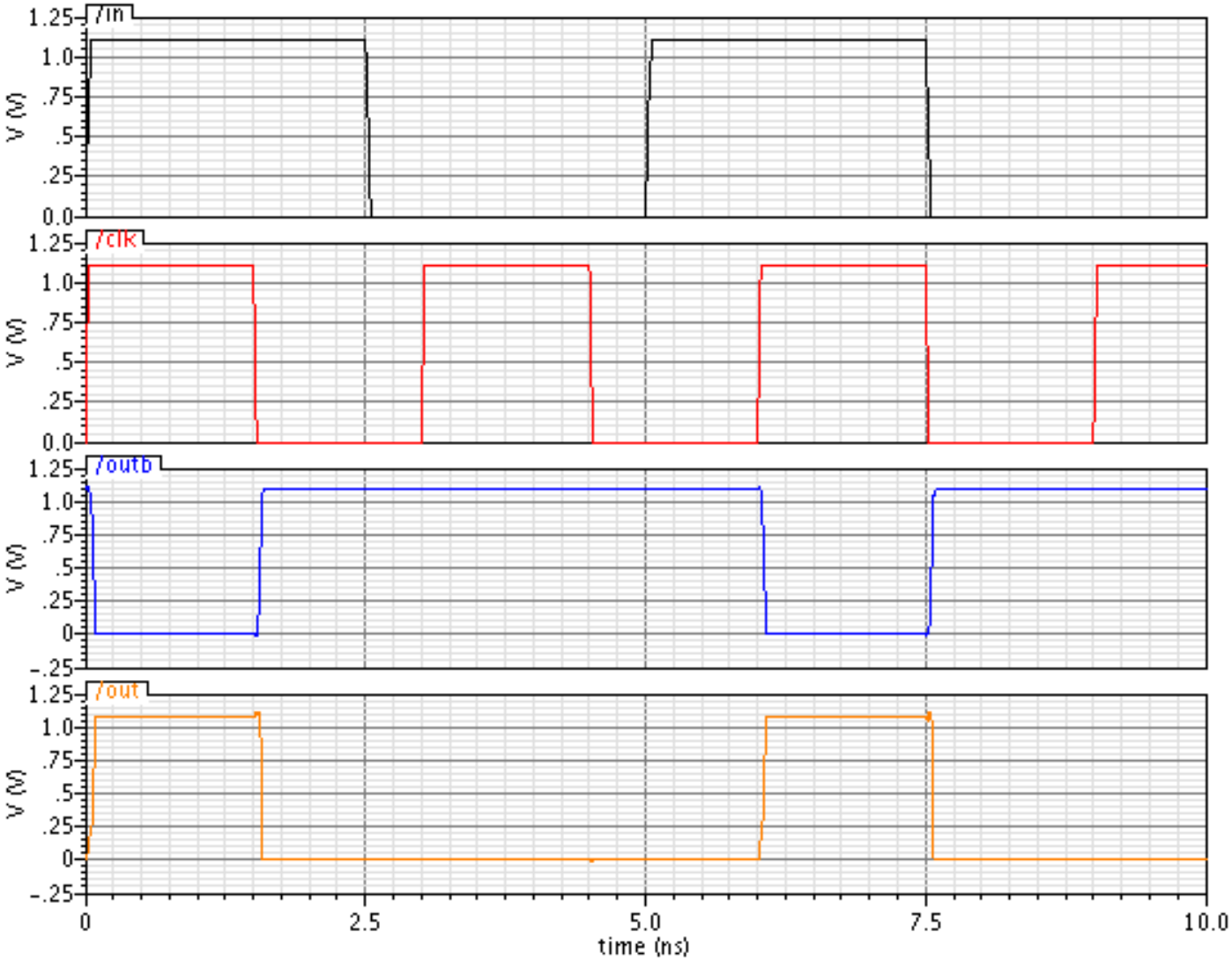

Figure 52 – Positive Edge Triggered Flip Flop Simulation

Negative Edge Triggered Flip Flop

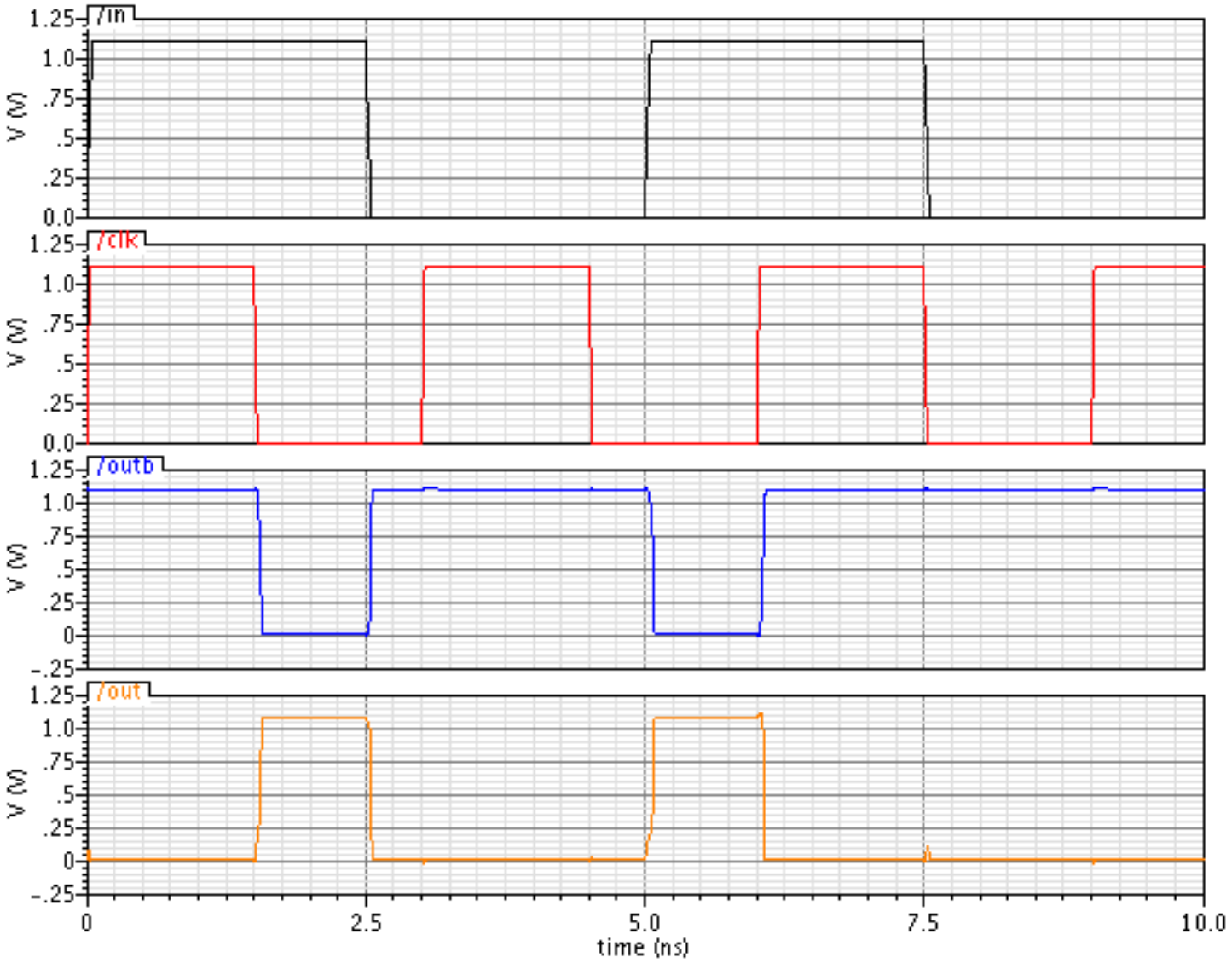

Figure 53 - Negative Edge Triggered Flip Flop Simulation